

June 2007 *Inside Edge*

Bringing you the latest Altera® product and solution news.

Monthly Spotlight

[Try Arria GX FPGAs with \\$995 development kit](#)

With the \$995 Arria™ GX development kit, you can design for PCIe, GbE & SRIO protocols, using proven Arria GX transceiver technology. The kit includes an Arria GX FPGA on a PCIe board, Quartus® II design software, reference designs, and demos. Order yours from the Altera eStore today!

FPGAs, CPLDs & Structured ASICs

[What could you create with a Cyclone III FPGA today?](#)

Now that Cyclone® III FPGAs are stocked on your distributor's shelves, you can produce anything from a four-channel H.264 encoder to a WiMAX pico-basestation. Take a look at our examples to help kick off your own designs today, then try them out in a low-cost Cyclone III development kit.

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Software, Intellectual Property & Development Kits

[Buy Quartus II Subscription software v7.1 online from eStore](#)

Quartus II Subscription Edition software v7.1 is now available to buy online. This Quartus II software offers support for high-end Stratix® FPGAs, advanced productivity features, a full license for popular DSP and memory controller IP functions, faster ModelSim® simulation, and more.

[From the Forum: Debug your FPGA design](#)

Have you exhausted your debug ideas and need some advice, like Altera Forum user **Bee Gee A**? See what users in the Forum suggested he try, then post your own tips, tricks, and questions today!

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Technology & End Markets

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Did You Know...

Which is the fastest car in production?

[Find out.](#)



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[Stratix III FPGAs: The only FPGAs with DDR3 SDRAM support](#)

Stratix III I/Os support the read and write leveling that is critical to successful DDR3 SDRAM design. The FPGAs' variable delay lines and dynamic on-chip termination increase margins as well as saving cost and power. Visit the Stratix III memory support center to learn more.

[SI Prescription with Dr. Bogatin: Got 12-port S-parameters?](#)

Long backplane channels are strongly dominated by losses and crosstalk, so 4-port differential S-parameters are not enough. To handle the crosstalk, 12 ports are preferred. Learn about the new 12-port vector network analyzer (VNA) and signal integrity from the SI Doctor, Dr. Eric Bogatin.

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Events, Training & Net Seminars

[QuickCast: Draining your battery's life: The myth of static Icc](#) **Free**

In just 10 minutes, see what some technical documents are hiding about static Icc. You'll learn the difference between static Icc and standby Icc, and why it matters in battery-powered applications. View the QuickCast today-- your battery will thank you for it!

[Training: Designing with the Nios II Processor and SOPC Builder](#)

In this course, you'll learn how to design in a soft 32-bit embedded processor. You'll compile designs with Quartus II and SOPC Builder software tools, and develop and run embedded software in the Nios® II IDE. Attendees get a 20% discount on a Nios II development kit!

[Webcast: Using PELE in the Stratix II GX design kit for HyperLynx](#)

Let Mentor Graphics and Altera take the fear out of implementing multi-gigabit link designs. This June 13 webcast will show you how to extract S-parameters from layouts in HyperLynx and to estimate Stratix II GX transceiver pre-emphasis and equalization settings in PELE.

[Register for Asia Pacific Technology Roadshow 2007](#) **Free**

July - Aug, Asia Pacific: Attend these technology-focused seminars to learn how Altera's DSP and transceiver-based interconnect technology solutions deliver unique value to different end markets. Seminar attendees can purchase Altera development boards at discounted price!

[Visit Altera at Europe's Largest EDA Industry Event!](#) **Free**

June 14-21, Germany, UK, Poland: Come and see Altera's newest technology at the EDA Tech Forums. These one-day events showcase the latest EDA trends, include panels with industry experts, offer breakout technology sessions focused on the hottest EDA topics. Register today!

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Support & Literature

[Interact with the FPGA using new In-System Sources & Probes \(PDF\)](#)

The new In-System Sources and Probes feature introduced in Quartus II software v7.1 allows you to use a JTAG connection to create virtual inputs into your design. Download the PDF to learn to create stimuli resulting in increased visibility in your debugging process.

[Tech Tip: How to apply MC exception for clock-enabled registers](#)

Applying multicycle (MC) exceptions based on clock enable is more productive than register-to-register MC constraints. Learn to create an MC exception constraint based off an enable register using Synopsys Design Constraint (SDC) commands.

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Altera in the News

[Altera attacks custom IC market to provide organic growth,](#)

EETimes Europe

Altera's Chairman and CEO, John Daane, believes that Altera will grow by 16% CAGR for the next few years, twice the estimated industry average. See how he plans to gain a bigger share of the ASIC market and make Altera the number one custom logic provider.

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Most Popular News from Last Issue

[Now Shipping: \\$199 Cyclone III FPGA Starter Kit](#)

Start your next low-power design with the low-cost Cyclone III FPGA Starter Kit. This kit is easy to use and includes everything you need to get started: development board with 25K LE FPGA, easy-to-use software, complete documentation, cables, and power supply. Order yours today!

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