

October 2007 *Inside Edge*

Bringing you the latest Altera® product and solution news.

Monthly Spotlight

[Download Quartus II Subscription Edition 30-Day Trial](#) **Free**

Download the new version of Quartus® II Subscription Edition software (v7.2) for a 30-day trial. Test the improved place-and-route algorithms and multi-processor support. You'll see 3X faster compile times and a 2-speed grade advantage against competing high-end 65-nm FPGAs.

FPGAs, CPLDs & Structured ASICs

[Reconfigure FPGA Transceivers On The Fly Without Downtime](#)

Tired of interrupting all your transceiver channels when you need to reconfigure just one? Now you can change protocols, data rates, and PMA settings without downtime! Use Stratix® II GX FPGAs, the only FPGAs with transceivers that support dynamic reconfiguration.

[Stratix III FPGAs: No Performance Degradation as Device Fills Up](#)

If performance is critical to your design, and your design uses much of the device's logic, your FPGA choice is even more important than usual. Learn how Stratix III and competing FPGAs stack up on large, ASIC-like designs, and how you can protect your performance margins.

[Build Your Cyclone III Design Right the First Time](#) (PDF)

Save time and avoid unnecessary headaches by using these insider tips on Cyclone® III design. This new app note covers it all--from choosing the right device to the final test. The design checklist at the end summarizes everything in one place for easy reference.

[Webcast: Learn How FPGAs Can Interface with DDR3 SDRAM](#) **Free**

In only two years, it's expected that implementing DDR2 will be more expensive than implementing DDR3. If you're starting a system design, you should consider DDR3 for its cost and power advantages. View this webcast to learn what's required in an FPGA to effectively implement DDR3.

[Webcast: Signal & Power Integrity Design Techniques for SSN](#) **Free**

In this 40-minute webcast, see how to improve the signal and power integrity on your system to minimize the effects of simultaneous switching noise (SSN). You'll see measured data on Stratix III design prototypes as well as simulation predictions. View the webcast today!

See New Device Availability

[Arria GX](#)
[Cyclone III](#)
[Stratix III](#)

Application Note:

Stratix III
Design Guidelines

Design Checklist



Did You Know...

Why a soft drink loses its fizz as it gets warm?
[Find out.](#)



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[Back to Top](#)

Software, Intellectual Property & Development Kits

[Run, Nios, Run! New Nios II Performance Benchmarks \(PDF\)](#)

The latest Nios® II benchmarks show Nios II /f processors running at 300 DMIPS in Stratix III FPGAs. See all the latest performance numbers and LE use for Nios II processor systems implemented in Stratix, Cyclone, and HardCopy® series devices. Download the data sheet today.

[Timing is everything! Analyze PLL timing in Quartus II software \(PDF\)](#)

Learn how to constrain and analyze the PLLs in your design using TimeQuest. You'll learn to model PLL clock jitter, skew, duty cycle distortion, and phase shift errors with the clock_uncertainty command. Learn to read the PLL timing reports in Quartus II software, and more.

[Back to Top](#)

Technology & End Markets

[SI Prescription with Dr. Bogatin: Smoothing on a Noisy Subject](#)

Take the guesswork out of designing complicated power distribution networks (PDNs) for your products. Learn about new interposers on the market that offer worry-free FPGA power delivery designs.

[White Paper: Design DSP Hardware with Catapult C Synthesis \(PDF\)](#)

Discover how Mentor Graphics' Catapult high-level C synthesis technology, used in combination with Altera accelerated libraries, gives designers a rapid path from algorithms modeled in C++ to optimized RTL running in Stratix III FPGAs for wireless and video applications.

[Back to Top](#)

Events, Training & Net Seminars

[Training: Interfacing to External Memory with Altera FPGAs](#)

Oct 23-Nov 30, various US locations: In this hands-on class, you'll learn about the design flows and options available when implementing external memory interfaces. You'll implement a DDR SDRAM controller, verify its functionality, connect your own logic, and close timing on your design.

[Video Series: Developing Software for the Nios II Processor](#) **Free**

Use this new series of video tutorials to learn how to develop software for the Nios II processor. Topics include a tools overview, debugging, software build flow, and more. Check out these training videos and get started on your next design today!

[Back to Top](#)

Support & Literature

[High-End 65-nm FPGA Architecture & Performance Comparison \(PDF\)](#)

At 65 nm, see how Stratix III FPGAs deliver the highest performance by leveraging its highly efficient 8-input fracturable LUT. Stratix III FPGAs not only deliver a 25% performance advantage over competing devices but also pack 1.8X more logic in the adaptive logic modules.

[From the Forum: Debug Tips for PLL Simulation Issues](#)

Altera Forum user **soalone** was able to simulate his PLL output in the Quartus II software, but unable to do it in ModelSim. Read the comments and suggestions from other Forum users that helped solve his problem, then post your own advice to gain some Forum reputation today!

[Design Example: Polyphase Modulation for Digital Up Conversion](#)

Conventional digital up converters modulate signals on carrier frequencies that are limited by the Nyquist theory. This design example avoids those limits by generating a carrier frequency that exceeds the NCO sampling frequency, easing requirements for analog modulation.

[Back to Top](#)

Altera in the News

[Customizing Multiservice Access Network Silicon, CommsDesign](#)

The entire network operation supply chain is investing in improving bandwidth, reliability, and scalability. See how FPGAs are at the forefront of this movement, including the rollout of MSAN equipment, and how access equipment manufacturers are using FPGAs for custom solutions.

[Back to Top](#)

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