

Welcome to the May issue of Altera's monthly Net Seminar e-Newsletter. Each issue gives you information on upcoming & recently broadcasted net seminars.

May 2005

Free Upcoming Net Seminars & Net Seminar Series



Register Now

[Improve Your Productivity in High-Density FPGA Designs](#)

Date: Wednesday, May 25, 2005

Time: 11:00 AM Pacific Time **Free**

Find out how Altera's Quartus® II software, including the industry's first incremental compilation technology, solves today's design challenges by dramatically reducing compilation times and improving productivity.

[Win a Gateway DVD Recorder \(US \\$250 Value\), Built With Altera Devices](#)



Register Now

[Reduce System Costs With Low-Cost Programmable Logic in Common Applications](#)

Date: Wednesday, June 8, 2005

Time: 11:00 AM Pacific Time **Free**

Learn about how Altera low-cost PLD solutions can reduce system costs and simplify design tasks while speeding time to market and extending product life at a surprisingly competitive price.

[Win a Gateway DVD Recorder \(US \\$250 Value\), Built With Altera Devices](#)

What Attendees Are Saying:

"Informative and reasonable in length, this [HardCopy® II Structured ASICs net seminar](#)

provided a convenient way to explore an attractive ASIC alternative."

Chris Reimer, Project Manager, Hewlett-Packard

Improve Productivity in High-Density FPGA Designs

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Recently Broadcasted Net Seminars & Net Seminar Series



[Power Solutions for Leading-Edge FPGAs](#)

Available Now! **Free**

[View Now](#)

This net seminar shows you how to mitigate FPGA power with appropriate thermal design, estimate power with tools, and compare various FPGAs with regards to power solutions.



[Accelerating Embedded System Designs With Soft-Core CPUs in FPGAs](#)

Available Now! **Free**

[View Now](#)

This net seminar describes how using FPGAs with soft-core processors, such as Altera's Nios® II embedded processors, can accelerate your system designs. In addition, the [Nios II development kit](#) is featured in an online demonstration to show you how quick and easy it is to implement multiple processors on a single chip.



HARDCOPY™ II

[View Now](#)

[Structured ASICs: A New Tool in the ASSP Developer's Tool Box](#)

Available Now! **Free**

As initial costs to develop a custom chip rise, ASSP companies in particular are finding that structured ASICs provide them with new business models for getting their intellectual property (IP) to market quickly and cost significantly less. The panel also discusses also cover the benefits structured ASICs offer start-up chip companies with the venture capital community.

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Congratulations





Eric Mastromarchi (left), a hardware engineer for Lucent Technologies, recently won a Gateway DVD Recorder, built with Altera devices, by viewing the [FPGA Power Solutions](#) net seminar live. Congratulations, Eric!

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