

Welcome to the August issue of Altera's monthly Net Seminar e-Newsletter. Each issue gives you information on upcoming and recently broadcasted net seminars.

August 2006

Free Upcoming Net Seminars & Net Seminar Series

[Optimizing High-Speed Serial Design Net Seminar Series](#)



3 sessions. Register Now! **Free**

**Partner Presenters:** Dr. Eric Bogatin, Cadence Design Systems

Discover why FPGAs with embedded transceivers are the ideal solution for the growing number of applications using high-speed, serial-based protocols. Learn how a complete solution, combined with good design practices and first-class EDA tools, can help reduce complexity and risk. [Register Now!](#)

Upcoming Net Seminar Series Highlights

<b>August 2, 2006</b> 11:00 AM PT	<b>Optimize Your High-Speed Board Design With Transceiver-Based FPGAs</b> <i>(Presented by Signal Integrity Expert Dr. Eric Bogatin &amp; Altera)</i> <i>Enter to win an Epson P-2000 Multimedia Storage Viewer (US\$500 value)</i>
<b>August 9, 2006</b> 11:00 AM PT	<b>Optimize Your PCB Layout With EDA Solutions</b> <i>(Presented by Cadence and Altera)</i> <i>Enter to win an Epson P-2000 Multimedia Storage Viewer (US\$500 value)</i>
<b>August 16, 2006</b> 11:00 AM PT	<b>Optimize Your High-Speed Protocol Implementation</b> <i>Enter to win an Epson P-2000 Multimedia Storage Viewer (US\$500 value)</i>

[Attend All for a Chance to Win an Altera Transceiver Signal Integrity Development Kit, Stratix® II GX Edition \(US\\$1,295\).](#)

"This 3-part [Embedded Net Seminar Series](#)

helped me learn more about the features and capabilities of Altera products. We are using Altera Stratix parts in our current designs and are looking at developing new features for future products. Their flexibility allows us to try some new ideas on our existing boards before we commit to our next product design."

Paul Bond, Hardware Engineer, GE



View any of the net seminars before September 30, 2006 and you will be eligible for a 50% discount on the Transceiver Signal Integrity Development

Kit, Stratix II GX Edition. [Register Now!](#)

## Recently Broadcast Net Seminars & Net Seminar Series



### [How to Protect Your IP Using FPGA Design Security](#)

View On-Demand Now! [Free](#)

The seminar describes how using FPGA design security lets you take advantage of the rich feature set and flexibility of high-density, high-performance FPGAs while protecting your intellectual property (IP).



### [Adding Triple-Play Test Capability Using FPGAs Net Seminar](#)

View On-Demand Now! [Free](#)

This net seminar describes the overall market and architectural trends for triple-play services and how testing OEM equipment capabilities is affected by the ever-changing development and deployment requirements carriers face.



### [Managing Signal Integrity for High-Speed Interfaces in FPGAs](#)

Available Now! [Free](#)

This seminar describes key elements of signal integrity and provides understanding of the eye-diagram and pass criteria of LVDS and memory-interface systems. The seminar also covers the LVDS and memory-interface signal integrity characterization results for Altera FPGAs.

Congratulations





Cisco Systems engineer Jason Reese won a Sony RDR-GX7 DVD recorder (US\$700 value) by viewing the net seminar titled [Addressing WiMAX Basestation Design Requirements Net Seminar](#). Congratulations, Jason!

---

As a subscriber to the Net Seminar e-Newsletter, you will receive a monthly email newsletter. Altera respects your privacy. If you no longer wish to receive this e-Newsletter, simply [unsubscribe](#).

[Subscribe](#) to additional Altera email updates and e-Newsletters, or view/edit all of your Altera email subscriptions. Other Altera email communications include:

- Product Announcements & Updates
- Inside Edge e-Newsletter
- Embedded e-Newsletter
- Code:DSP e-Newsletter

Copyright© 1995-2006 Altera Corporation, 101 Innovation Drive, San Jose, California 95134, USA