

January 2007: Altera's net seminar monthly e-newsletter provides schedules and descriptions of upcoming and recently broadcast Altera® online seminars.

You've heard about Stratix III FPGAs. Now find out what the buzz is about.



[Overview of Altera's 65-nm Stratix III FPGAs](#) **Free**

Duration: 15 minutes
View On-Demand Now!

In this QuickCast, Jordon Plofsky, Altera's Senior Vice President of Marketing, and Brad Howe, Altera's Vice President of IC Design Engineering, discuss how Altera's Stratix® III 65-nm high-end FPGAs meet product and engineering management's business and technical requirements.

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[Using Stratix III FPGAs to Achieve Higher Performance Systems with Lower Power](#) **Free**

Duration: 60 minutes
View On-Demand Now!

Design your next-generation high-end system with confidence. Learn how Stratix III FPGAs, with Programmable Power Technology, deliver maximum power when needed to performance critical paths in the design, and low power everywhere else. Discover how the use of performance-optimizing Quartus® II development tools and EDA synthesis support provide complete solutions for high-end system design.

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["The Code:DSP - Video, Image, and Signal Processing Net Seminar Series](#)

is extremely helpful After seeing the seminars for the DSP: Video, Image and Signal Processing, I have a better understanding of which Altera product to use and what partner company to work with that will produce a system with the minimal amount of integration time."

- Brandon Gushiken,
Engineer, Trex Hawaii





[Learn Best Board Design Practices for Power Delivery Network](#) **Free**

Duration: 60 minutes
View On-Demand Now!

For a high level of system signal integrity, you need a robust power delivery network (PDN). In this net seminar, the SI Doctor, Dr. Eric Bogatin, provides detailed practical strategies for achieving low PDN impedance. He covers voltage regulator modeling and simulations; techniques to estimate and achieve PDN target impedance; the proper selection of decoupling capacitors; and more.

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[Learn About High-Speed Clocking Architecture and Oscillator Selection](#) **Free**

Duration: 60 minutes
View On-Demand Now!

There's little room for clock uncertainties and variations in high-speed or wide-bus interfaces, such as gigabit transceiver or high-speed memory interfaces. This net seminar covers various clock network topologies for FPGAs as well as a detailed discussion of jitter, its components and causes. Finally, guidelines are provided for how to select the right oscillator for your high speed design.

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Congratulations



Representing Altera, Gord Leddy of Future California Electronics, presents Dennis Cote, Harding Instruments engineer, an Epson P-2000 Multimedia Viewer (\$500 US). Dennis won it by attending the net seminar, [Learn Best Board Design Practices for Power Delivery Network](#).



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