

Quartus II Software Advantages for MAX+PLUS II Software Users



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The Altera® Quartus® II development software, which provides advanced features and a comprehensive environment for system-on-a-programmable-chip (SOPC) design, is now the preferred design tool for all Altera devices. Using the Quartus II software can increase productivity by shortening design and verification cycles.

The Quartus II software supports all Altera FPGA device families, including Stratix™, Stratix GX, and Cyclone™ devices. This technical brief explains the benefits of using the Quartus II software for MAX+PLUS II® designs and any new design targeting Altera devices. Topics discussed include:

- Quartus II software exclusive features
- Design file compatibility & importing assignments
- Comparing MAX+PLUS II and Quartus II Software Procedures
- Software requirements
- Device support

Quartus II Software Exclusive Features

The Quartus II software provides access to many productivity-enhancing features not available with the MAX+PLUS II software. If you are using FLEX and MAX devices, you can now take advantage of the Quartus II software's exclusive features, including:

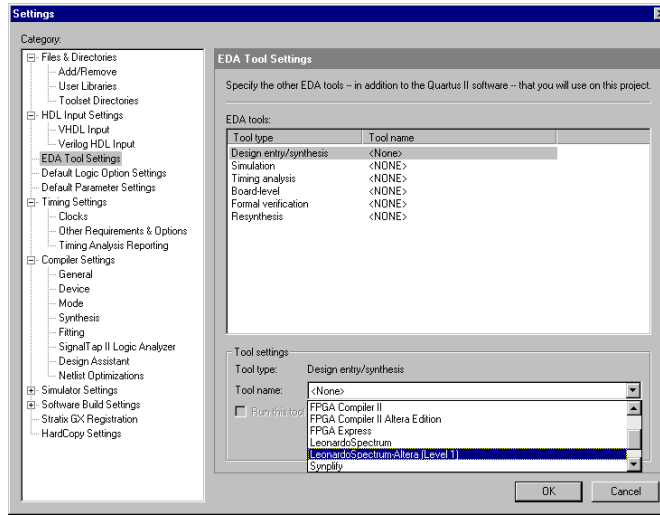
- NativeLink® integration
- Creating Hardware Description Language (HDL) files from schematic Block Design Files (.bdf)
- Design compilation enhancements
- Multiple clock & multi-cycle timing analysis
- Slack reporting
- Tool command language (Tcl) scripting support

The following sections highlight these features.

NativeLink Integration

The Quartus II software features NativeLink integration, providing seamless data transfer with major third-party EDA tools. This NativeLink integration allows the Quartus II software to easily identify the source of any errors in the EDA tool's source files, enabling you to correct them quickly. In addition, the Quartus II software allows you to run many EDA tools automatically from within the Quartus II software, further enhancing its design flow integration. Figure 1 shows the **EDA Tool Settings** dialog box (Assignments menu).

Figure 1. EDA Tool Settings Dialog Box



For detailed information on using NativeLink integration, go to “EDA Interfaces” in the Quartus II Help. The Quartus II Help provides comprehensive documentation for the Quartus II software, as well as a general tutorial. To launch the Quartus II Help, press the F1 key when you are working in the Quartus II software graphical user interface.

Creating HDL Files from Block Design Files

The Quartus II software allows you to convert BDFs into VHDL or Verilog HDL files for synthesis and simulation in other EDA tools. This feature is available exclusively in the Quartus II software.



For detailed information on using this conversion feature, go to “Create HDL Design File for Current File command” in the Quartus II Help.

Design Compilation Enhancements

The fast fit feature of the Quartus II software shortens compilation times by up to 50%, with a minimal (5%) impact on design performance. This feature is ideal for running multiple iterations early in the design cycle, and can be turned off to meet final performance goals if necessary. This feature is available for designs targeting look-up table- (LUT-) based devices. To enable this feature, go to the **Fitting** tab in the **Settings** dialog box (Assignments menu).



For details on the fast fit compilation option, go to “Increasing Compilation Speed with Fast Fit” in the Quartus II Help. For more information on adjusting the compilation level and compilation speed/disk usage trade-off for your design, see “Compiler Settings Command” in the Quartus II Help.

Multiple Clock & Multi-Cycle Timing Analysis

The Quartus II software performs timing analysis for multiple clock settings and multi-cycle timing assignments. For example, the Quartus II software can perform multiple clock timing analysis across multiple clock domains to provide an accurate result of your design performance. Conversely, MAX+PLUS II timing analysis is restricted to single clock domains.



For more information on timing analysis, go to “Overview: Using the Timing Analyzer” in the Quartus II Help, or refer to *Application Note 123 (Using Timing Analysis in the Quartus II Software)*.

Slack Reporting

Slack is the time margin by which a timing requirement was met or not met, which commonly occurs in designs with strict timing requirements or complex timing assignments. The Quartus II software determines slack with the following equation:

$$\text{Slack} = (\text{Required clock period}) - (\text{Actual clock period})$$

A positive slack value, which the Quartus II software displays in black, indicates the margin by which a requirement was met. A negative slack value, which the Quartus II software displays in red, indicates the margin by which a requirement was not met.

The Quartus II Timing Analyzer reports timing analysis results as slack values in the Clock Requirement, Clock Setup Time (t_{SU}) Requirements, Clock Hold Time (t_H) Requirements, Clock-to-Output Delay (t_{CO}) Requirements, Pin-to-Pin Delay (t_{PD}) Requirements, t_{PD} Minimum Requirements, and/or Minimum Setup & Hold Requirement sections of the Compilation Report.



For more information on slack, refer to *AN 123: Using Timing Analysis in the Quartus II Software*.

Tcl Scripting Support

In the Quartus II software, you can execute Tcl commands or create and run Tcl scripts to perform many operations in a Quartus II project, such as making assignments, running compilations and simulations, and performing timing analysis. The Quartus II software can generate a Tcl script to compile an existing project and provides Tcl templates to enable creating custom scripts to automate design flows.



For details on Tcl scripting support, go to “Tcl: Overview Topics” in the Quartus II Help.

Design File Compatibility & Importing Assignments

You can easily compile existing MAX+PLUS II-based FLEX and MAX design files in the Quartus II software. If you have project assignments, an automated process translates them from the MAX+PLUS II Assignment and Configuration File (.acf) format into the Quartus II settings and configuration file format (.esf and .csf). The **New Project Wizard** (File menu) can assist you in setting up your Quartus II project.

Comparing MAX+PLUS II and Quartus II Software Procedures


Compiling a design using the Quartus II software is as simple as with the MAX+PLUS II software. The tables in this section show design procedures using the MAX+PLUS II version 10.1 and higher software alongside the equivalent procedures using the Quartus II version 2.2 and higher software.

Table 1 compares the respective procedures in the MAX+PLUS II software and Quartus II software used to initially set-up a project.

Table 1. Project Set-Up Comparison

MAX+PLUS II	Quartus II
1. Choose Project-Name (File menu).	1. Choose New Project Wizard (File menu). After reading the introduction, click Next .
2. Specify the project name and project directory containing design files. Click OK . (The project name must be the same as the top-level design file name.)	2. Specify the working directory, project name, and top-level entity. Click Next .
3. If necessary, choose EDA Netlist Reader Settings (Interfaces menu) and click Vendor to specify required library mapping file.	3. Specify design files and libraries, if necessary. Click Next .
4. Choose Device (Assign menu) to specify target Altera device.	4. If necessary, select EDA tools and confirm or specify required library mapping files for synthesis tools. Click Next .
5. Choose Compiler (MAX+PLUS II menu) and click Start to launch a compilation.	5. Specify device family and choose Yes . Choose to specify a specific device or to allow the Compiler to do so, and click Next .
	6. Under Filter , make selections in from the Package , Pin Count , and Speed Grade lists to refine the list of specific devices that can be selected for the project.
	7. Click Next to view a summary of your settings then click Finish to exit the Wizard then select Start Compilation (Processing menu) to begin a compilation.

Altera recommends having different directories for different projects using the Quartus II software.

 To import MAX+PLUS II assignments to the Quartus II setting and configuration file format (.esf and .csf), select **Import MAX+PLUS II Assignments** (Assignments menu). The Quartus II and MAX+PLUS II software formats for node names and bus pin names are schematically different. Make sure that the naming schemes map properly and do not interfere with design logic (see Table 2).

Feature	Quartus II Format	MAX+PLUS II Format
Node name	auto_max:auto q0	Auto_max:auto q0
Pin name	d[0], d[1], d[2]	d0, d1, d2

The Import MAX+PLUS II Assignments feature in the Quartus II software inserts square brackets around the ending number of all pin names representing a bus of pin signals. However, if your design has pin names ending in numbers that are not part of a bus, you may need to manually remove the square brackets from the Quartus II settings and configuration for the assignments to be valid during the Quartus II design compilation.

The MAX+PLUS II software implements “Cut Timing Paths” assignments for all paths feeding and being fed by the selected node names. When importing these assignments into the Quartus II software, this assignment only applies to all paths being fed by the selected node names. Use the Quartus II Assignment Organizer (Assignments menu) to implement the Cut Timing Paths assignment to paths feeding the selected node name.

Timing Analysis Comparison

The Quartus II software performs timing analysis automatically during compilation of the design. Table 2 compares the respective procedures in the MAX+PLUS II software and Quartus II software used for timing analysis.

Table 3. Comparing Timing Analysis Procedures Used in the MAX+PLUS II and Quartus II Software

MAX+PLUS II	Quartus II
1. To view results of setup and hold time analysis, choose Setup/Hold Matrix (Analysis menu), and click Start .	1. Expand the Timing Analyses folder of the Compilation Report to view the results. The tsu and th sections display the clock setup and hold times of every input register. The tco section displays the clock-to-output delay of every output register.
2. To view the worst-case registered performance as given by the minimum required clock period and the maximum clock frequency for every clock signal in the circuit, choose Delay Matrix (Analysis menu), and click Start .	The fmax section displays the frequency requirements and reports the worst-case speed performance of the specified clock signal.
3. To view results of propagation delays, from the Analysis menu, choose Delay Matrix (Analysis menu), and click Start .	The tpd section displays the longest and shortest point-to-point delay between the source and destination nodes.

Simulation Comparison

Table 4 compares the respective procedures in the MAX+PLUS II software and Quartus II software used to initially set-up a project.

Table 4. Comparing Simulation Procedures Used In MAX+PLUS II and Quartus II

MAX+PLUS II	Quartus II
1. Choose Waveform Editor (MAX+plus II menu) to create a new Simulator Channel File (SCF) for the Waveform Editor.	1. Choose New (File menu). Click the Other Files tab. Select Vector Waveform File (.vwf), and click OK.
2. Choose Insert Node (Node menu) to specify nodes for simulation. You can also choose Enter Nodes from SNF (Node menu) to specify nodes from the Simulator Netlist File (SNF) which is generated during compilation.	2. Choose Utility Windows > Node Finder (View menu). Select nodes for simulation and drag the node names to your VWF.
3. Choose Save (File menu) to save the SCF file.	3. Choose Save (File menu) to save the VWF file.
4. Choose Simulator (MAX+PLUS II menu) and click Start Simulation . The results are reported in the SCF file.	4. Choose Run Simulation (Processing menu). Stimulus is retained in the VWF and simulation results are displayed in the Simulation Report window.

Viewing MAX+PLUS II SCF Files in the Quartus II Software

To view MAX+PLUS II SCF files in the Quartus II software, save the SCFs as Table Files (.tbl) in the MAX+PLUS II software. Then open the Table File using the Quartus software and save it as a VWF.

To create a Table File in the MAX+PLUS II Waveform Editor, perform the following steps:

1. Choose **Create Table File** (File Menu). The Create Table File dialog box is displayed.
2. Select an existing filename in the Files box, or type a filename in the File Name box. The filename may contain up to 32 name characters. If you do not specify an extension, the extension .tbl is automatically appended to the filename. Choose **OK**.
3. In the Quartus II software, choose **Open** (file menu) and select the table file saved in step 3.
4. Save the file in Quartus II as a VWF.

When reading Table Files that contain groups and buses into the Quartus II software, the bracket notation, or bus names, may not be recognized by the Quartus II software during simulation. To avoid this problem, re-extract the group name or individual bits from the Quartus II Node Finder and paste the new waveform to correspond to the newly created node names.

Programming Comparison

Table 5 compares the respective procedures in the MAX+PLUS II software and Quartus II software used to begin programming.

Table 5. Comparing Programming Procedures Used in the MAX+PLUS II and Quartus II Software

MAX+PLUS II	Quartus II
1. From the MAX+PLUS II menu, choose Programmer .	1. Choose Programmer (Tools menu.)
2. From the Options menu, choose Hardware Setup to specify Programming Hardware.	2. Click setup in the Programming Hardware section to specify programming hardware.
3. From the File menu, choose Select Programming File to select a programming file. Click OK . Click Program to start programming.	3. Click Add File to add programming files. Click OK . Select Program/Configure for the desired programming files. Click Start .

Software Requirements

Operating system requirements are the same for both the Quartus II software and MAX+PLUS II software. Customers on active subscription receive license files and CD-ROMs that enable both the Quartus II and the MAX+PLUS II software.

Devices Supported

The Quartus II software supports the FLEX and MAX device families in addition to the APEX™ II, APEX 20K, Mercury™, Excalibur™, Stratix, and Cyclone device families. Table 6 shows device support for both the Quartus II and the MAX+PLUS II design software.

Table 6. Devices Supported by the Quartus II & MAX+PLUS II Software	
Development Tool	Devices Supported
Quartus II	Cyclone, Stratix, Stratix GX, Excalibur, Mercury, APEX II, APEX 20KE, APEX 20KC, ACEX 1K, FLEX 6000, FLEX 10KE, MAX 7000B, MAX 7000AE, and MAX 3000A
MAX+PLUS II	ACEX 1K, FLEX 6000, FLEX 10KE, MAX7000S, MAX 7000B, MAX 7000AE, and MAX 3000A

Further Information

For a good overview of the Quartus II software, Choose Contents (Help menu). The procedures described in this technical brief are more fully explained in the following sections of the help system:

- Starting Projects
- Compiling a Design

- Viewing and Using Timing Analysis
- Simulating a Design
- Programming or Configuring a Device
- Device Support

The Quartus II software's help system also includes a comprehensive tutorial to walk you through creating a project and performing common design, synthesis, place-and-route, and verification tasks. The tutorial also includes advanced sections which cover using LogicLock™ block-based design flow and designing for Stratix™ and Excalibur™ devices to help you quickly master designing with the latest devices and methodologies.

Conclusion

The Quartus II software provides new and advanced features for designs targeting all Altera device families. MAX+PLUS II software users can use the Quartus II software to continue current designs for these devices with no need to modify or convert the current design files. While providing support for MAX and FLEX devices, Quartus II also allows design for Altera's newest device families including Stratix, Stratix GX, and Cyclone.



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