PowerPlay Early Power Estimator

User Guide for Arria II GX FPGAs

101 Innovation Drive
San Jose, CA 95134
www.altera.com

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1. About the Arria II GX PowerPlay Early Power Estimator

Release Information

Table 1–1 provides information on the version of the PowerPlay Early Power Estimator spreadsheet documented in this User Guide.

Table 1–1. PowerPlay Early Power Estimator Spreadsheet Versions

Device Family	PowerPlay Early Power Estimator Spreadsheet Version
Arria® II GX	9.0 and later

Device Family Support

The PowerPlay Early Power Estimator spreadsheet provides support for the target Altera® device families listed in Table 1–2.

Table 1–2. Device Family Support

Device Family	Support
Arria II GX	Preliminary

General Description

Printed circuit board (PCB) designers need an accurate estimate of the amount of power a device consumes to develop an appropriate power budget, design the power supplies, voltage regulators, heat sink, and cooling system. You can calculate a device's power using the Microsoft® Excel®-based PowerPlay Early Power Estimator spreadsheet available from the Altera website (www.altera.com) or the PowerPlay Power Analyzer in the Quartus® II software. Enter the device resources, operating frequency, toggle rates, and other parameters in the spreadsheet to use the PowerPlay Early Power Estimator.

This User Guide explains how to use the PowerPlay Early Power Estimator spreadsheet to estimate device power consumption.

☞ You should only use these calculations as an estimation of power, not as a specification. Be sure to verify the actual power during device operation, as the information is sensitive to the actual device design and the environmental operating conditions.

For more information about available device resources, I/O standard support, and other device features, refer to the appropriate device family handbook.

Features

The features of the PowerPlay Early Power Estimator spreadsheet include:

- Estimate your design's power usage before creating the design or during the design process
- Import device resource information from the Quartus II software into the PowerPlay Early Power Estimator spreadsheet with the use of the Quartus II-generated PowerPlay Early Power Estimator file
- Perform preliminary thermal analysis of your design

2. Setting Up the Arria II GX PowerPlay Early Power Estimator

System Requirements

The PowerPlay Early Power Estimator spreadsheet requires:

- A personal computer (PC) running the XP/Vista operating system
- Microsoft® Excel® 2003 (US version) or higher
- Quartus® II software version 9.0 or higher (if generating a file for import)

Download and Install the PowerPlay Early Power Estimator

The PowerPlay Early Power Estimator spreadsheet for Altera® devices is available from the Altera website (www.altera.com). After reading the terms and conditions and clicking **I Agree**, you can download the Microsoft Excel file to your hard drive.

By default, the Microsoft Excel 2003 macro security level is set to high. When the macro security level is set to high, macros are automatically disabled. To change the macro security level in Microsoft Excel 2003, click **Options** on the Tools menu. On the **Security** tab of the Options window, click **Macro Security**. On the **Security Level** tab of the **Security** dialog box, choose **Medium**. When the macro security level is set to **Medium**, a pop-up window asks you whether to enable macros or disable macros each time you open a spreadsheet that contains macros. After changing the macro security level, you must close the spreadsheet and re-open it in order to use the macros.

Estimating Power

You can estimate power at any point in your design cycle. You can use the PowerPlay Early Power Estimator spreadsheet to estimate the power consumption if you have not begun your design, or if your design is not complete. While the PowerPlay Early Power Estimator spreadsheet can provide you with an estimate for your complete design, Altera highly recommends you use the PowerPlay Power Analyzer in the Quartus II software to obtain this estimate. In general, using the PowerPlay Power Analyzer in the Quartus II software should be your preferred method of generating power estimates because it knows your exact routing and various modes of operation.

For more information about the power estimation feature in the Quartus II software, refer to the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

To use the PowerPlay Early Power Estimator, enter the device resources, operating frequency, toggle rates, and other parameters in the PowerPlay Early Power Estimator. If you do not have an existing design, you need to estimate the number of device resources your design uses in order to enter the information into the PowerPlay Early Power Estimator.

Estimating Power before Starting the FPGA Design

FPGAs provide the convenience of a shorter design cycle and faster time-to-market than ASICs or ASSPs. This means that the board design often takes place concurrent with the FPGA design cycle. Thus, power planning for the device can happen before any of the FPGA design is complete.

Table 2–1 shows the advantages and disadvantages of using the PowerPlay Early Power Estimator spreadsheet before you begin the FPGA design.

Table 2–1. Power Estimation Before Designing the FPGA Device

Advantages	Disadvantages
■ Power estimation can be done before starting your FPGA design	■ Accuracy depends on your inputs and your estimation of the device resources; where this information may change (during or after your design is complete), your power estimation results may be less accurate ■ Process can be time consuming

Use the following steps to estimate power usage with the PowerPlay Early Power Estimator spreadsheet if you have not started your FPGA design:

1. Download the PowerPlay Early Power Estimator spreadsheet from the Altera website (www.altera.com).
2. Select the target family, device, and package from the PowerPlay Early Power Estimator's **Family**, **Device**, and **Package** sections.
3. Enter values for each section in the PowerPlay Early Power Estimator. Different worksheets in the file display different power sections, such as clocks and phase-locked loops (PLLs). Power is calculated automatically and subtotals are given for each section.
4. The calculator displays the estimated power usage in the **Total** section.

Estimating Power While Creating the FPGA Design

When the FPGA design is partially complete, you can use the PowerPlay Early Power Estimator file (<*revision name*>**_early_pwr.csv**) generated by the Quartus II software to supply information to the PowerPlay Early Power Estimator. After importing the power estimation file information into the PowerPlay Early Power Estimator, you can edit the PowerPlay Early Power Estimator spreadsheet to reflect the device resource estimates for the final design.

For more information about generating the power estimation file in the Quartus II software, refer to the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

Table 2–2 shows the advantages and disadvantages when using the PowerPlay Early Power Estimator spreadsheet for an FPGA design that is partially complete.

Table 2–2. Power Estimation When the FPGA Design is Partially Complete

Advantages	Disadvantages
■ Power estimation can be done early in the FPGA design cycle ■ Provides the flexibility to automatically fill in the PowerPlay Early Power Estimator spreadsheet based on the Quartus II software compilation results	■ Accuracy depends on your inputs and your estimation of the device resources; where this information may change (during or after your design is complete), your power estimation results may be less accurate

Use the following steps to estimate power usage with the PowerPlay Early Power Estimator spreadsheet if your FPGA design is partially complete:

1. Compile the partial FPGA design in the Quartus II software.
2. Generate the PowerPlay Early Power Estimator file (<*revision name*>**_early_pwr.csv**) in the Quartus II software by clicking **Generate PowerPlay Early Power Estimator File** on the Project menu.
3. Download the PowerPlay Early Power Estimator spreadsheet from the Altera website (www.altera.com).
4. Import the PowerPlay Early Power Estimator file into the PowerPlay Early Power Estimator spreadsheet to automatically populate the PowerPlay Early Power Estimator spreadsheet entries.
5. After importing the file to populate the PowerPlay Early Power Estimator, you can manually edit the cells to reflect final device resource estimates.

Estimating Power after Completing the FPGA Design

When you complete your FPGA design, the PowerPlay Power Analyzer in the Quartus II software provides the most accurate estimate of device power consumption. The PowerPlay Power Analyzer uses simulation, user mode, and default toggle rate assignments, in addition to place-and-route information, to determine power consumption. Altera strongly recommends that you use the PowerPlay Power Analyzer when your FPGA design is complete.

For more information about how to use the PowerPlay Power Analyzer in the Quartus II software, refer to the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

Entering Information into the PowerPlay Early Power Estimator

You can either manually enter power information into the PowerPlay Early Power Estimator spreadsheet or load a PowerPlay Early Power Estimator file generated by the Quartus II software, version 9.0 or higher. You can also clear all the values currently in the PowerPlay Early Power Estimator.

Clearing All Values

You can reset all the user-entered values in the PowerPlay Early Power Estimator spreadsheet by clicking **Reset**.

To use the **Reset** feature, you must enable macros for the spreadsheet. If you have not enabled macros for the spreadsheet, you need to reset all user-entered values manually.

Manually Entering Information

You can manually enter values into the PowerPlay Early Power Estimator spreadsheet in the appropriate section. White, unshaded cells are input cells and may be modified. Each section contains a column that allows you to specify a module name based on your design.

Importing a File

If you already have a partially completed design, the PowerPlay Early Power Estimator file generated by the Quartus II software contains the device resource information. You can import the PowerPlay Early Power Estimator file into the PowerPlay Early Power Estimator. Importing a file saves you time and effort otherwise spent manually entering information into the PowerPlay Early Power Estimator. You can also manually change any of the values after importing a file.

To generate the PowerPlay Early Power Estimator file, you must first compile your design in the Quartus II software. After compiling the design, click **Generate PowerPlay Early Power Estimator File** on the Project menu. The Quartus II software creates a PowerPlay Early Power Estimator file with the name <*revision name*>**_early_pwr.csv**.

For more information about generating the PowerPlay Early Power Estimator file in the Quartus II software, refer to the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

To import data into the PowerPlay Early Power Estimator, perform the following steps:

1. Click **Import Quartus II File** in the PowerPlay Early Power Estimator.
2. Browse to a power estimation file generated from the Quartus II software and click **Open**. The file has a name <*revision name*>**_early_pwr.csv**.
3. Click **OK** in the confirmation window to proceed.
4. When the file is imported, click **OK**. Clicking **OK** acknowledges the import is complete. If there are any errors during the import, an **.err** file is generated with details.

After importing a file, you must verify all your information.

Importing a file from the Quartus II software populates all input parameters on the Main page that were specified in the Quartus II software. These parameters include:

- Family
- Device
- Package
- Temperature grade
- Power characteristics
- Ambient or junction temperature
- Heat sink
- Airflow
- Custom θ_{SA} or custom θ_{JA}
- Board thermal model

The ambient or junction temperature, heat sink, airflow, custom θ_{SA} or custom θ_{JA}, and board thermal model parameters are optional. See "Main Input Parameters" on page 9 for more information about these parameters.

The f_{MAX} values imported into the PowerPlay Early Power Estimator spreadsheet are the same as the f_{MAX} values specified by the designer in the Quartus II software. You can manually edit the f_{MAX} and the toggle percentage in the PowerPlay Early Power Estimator spreadsheet to suit your system requirements.

3. Using the Arria II GX PowerPlay Early Power Estimator

Introduction

The PowerPlay Early Power Estimator spreadsheet provides the ability to enter information into sections based on architectural features. The PowerPlay Early Power Estimator spreadsheet also provides a subtotal of power consumed by each architectural feature and is reported in each section in watts (W).

PowerPlay Early Power Estimator Inputs

The following sections of this user guide explain what values you need to enter for each section of the PowerPlay Early Power Estimator. The different Excel® worksheets of the PowerPlay Early Power Estimator spreadsheet are referred to as sections. Sections in the PowerPlay Early Power Estimator spreadsheet calculate power representing architectural features of the device, such as clocks, RAM blocks, or digital signal processing (DSP) blocks.

Main Input Parameters

Different devices consume different amounts of power for the same design. The larger the device, the more power it consumes because of the larger die and longer interconnects in the device.

In the **Main** section, you may enter the following parameters for the device and design:

- Family
- Device
- Package
- Temperature grade
- Power characteristics
- Ambient or junction temperature
- Heat sink used
- Airflow
- Custom heat sink information
- Board thermal model

☞ Parameters required depend on whether the junction temperature is entered manually or auto computed.

Table 3–1 describes the values that need to be specified in the **Main** section of the PowerPlay Early Power Estimator.

Table 3–1. Main Section Information (Sheet 1 of 2)

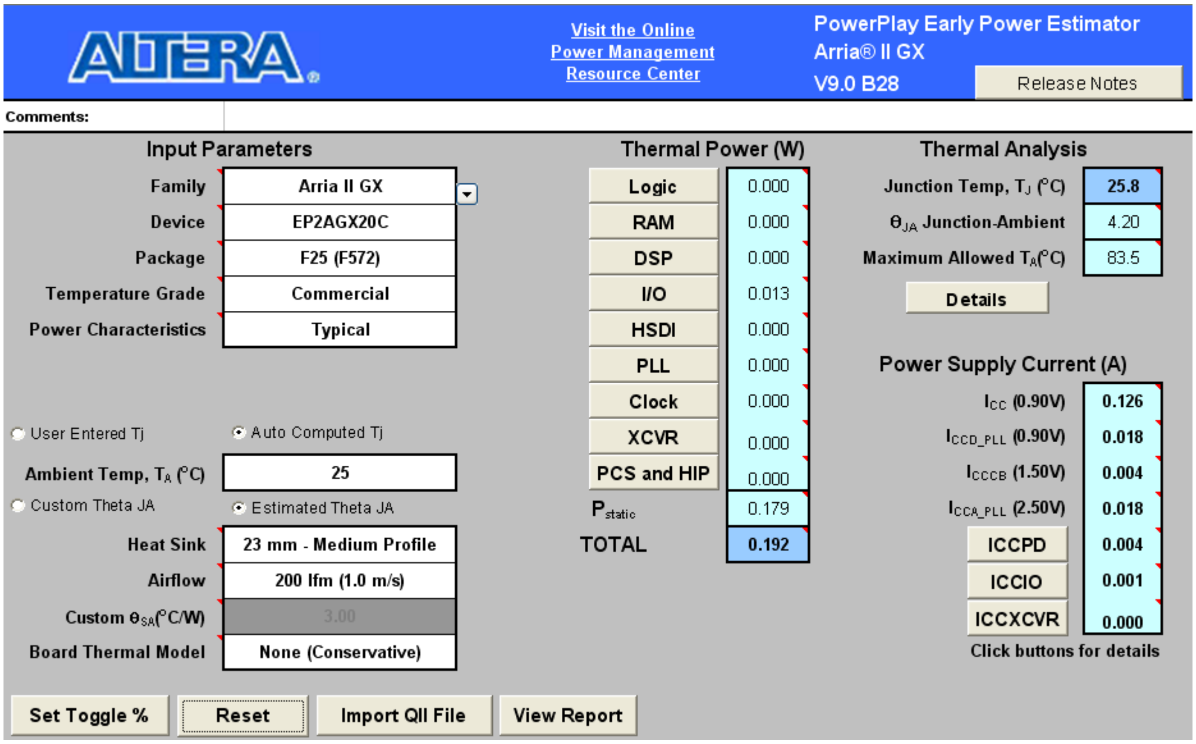
Input Parameter	Description
Family	Select the device family. Only the Arria® II GX family is available.
Device	Select your device. Larger devices consume more static power and have higher clock dynamic power. All other power components are unaffected by device.
Package	Select the package that is used. Larger packages provide a larger cooling surface and more contact points to the circuit board, leading to lower thermal resistance. Package selection does not affect dynamic power.
Temperature Grade	Select the appropriate temperature grade. Currently, only commercial devices are available for Arria II GX devices. Commercial devices have a maximum operating temperature of 85°C. This field only affects the maximum junction temperature.
Power Characteristics	Select the typical or theoretical worst-case silicon process. Currently, only the typical silicon process is available for the Arria II GX device. There is process variation from die-to-die. This primarily impacts static power consumption. **Typical** provides results that line up with average device measurements.
Junction Temp, T_J (°C)	Enter the junction temperature of the device. This value can range from 0°C to 85°C for commercial grade devices and -40°C to 100°C for industrial grade devices. This field is only available when you select **User Entered T_J**. In this case, junction temperature is not calculated based on the thermal information provided.
Ambient Temp, T_A (°C)	Enter the air temperature near the device. This field is only available when you select **Auto Computed T_J**. If you select **Estimated Theta J_A**, this field is used to compute junction temperature based on power dissipation and thermal resistances through the top-side cooling solution (heat sink or none) and board (if applicable). If you select **Custom Theta J_A**, this field is used to compute junction temperature based on power dissipation and the custom θ_{JA} entered.
Heat Sink	Select the heat sink being used. You can specify no heat sink, a custom solution, or specify a heat sink with set parameters. This field is only available when you select **Auto Computed T_J** and **Estimated Theta J_A**. Representative examples of heat sinks are provided. Larger heat sinks provide lower thermal resistance and thus lower junction temperature. If the heat sink is known, consult the heat sink data sheet and enter a Custom heatsink-to-ambient value according to the airflow in your system. The heat sink selection updates θ_{SA} and the value is seen in the Custom θ_{SA} (°C/W) parameter. If you select a custom solution, the value is what is entered for Custom θ_{SA} (°C/W).

Table 3–1. Main Section Information (Sheet 2 of 2)

Input Parameter	Description
Airflow	Select an available ambient airflow in linear-feet per minute (lfm) or meters per second (m/s). The options are 100 lfm (0.5 m/s), 200 lfm (1.0 m/s), 400 lfm (2.0 m/s), or still air. This field is only available when you select **Auto Computed T_J** and **Estimated Theta J_A**. Increased airflow results in a lower case-to-air thermal resistance and thus lower junction temperature.
Custom θ_{JA} (°C/W)	Enter the junction-to-ambient thermal resistance between the device and ambient air (in °C/W). This field is only available when you select **Auto Computed T_J** and **Custom Theta J_A**. This field represents the increase between ambient temperature and junction temperature for every Watt of additional power dissipation.
Custom θ_{SA} (°C/W)	Enter the heatsink-to-ambient thermal resistance from the heat sink data sheet if you select a custom heat sink. The quoted values depend on system airflow and may also depend on thermal power dissipation. This field is only available when you select **Auto Computed T_J**, **Estimated Theta J_A**, and if you set the Heat Sink parameter to **Custom Solution**. The Custom θ_{SA} parameter is combined with a representative case-to-heatsink resistance and an Altera-provided junction-to-case resistance to compute overall junction-to-ambient resistance through the top of the device.
Board Thermal Model	Select the type of board to be used in thermal analysis. The value can either be **None (Conservative)**, **JEDEC (2s2p)**, or **Typical Board**. This field is only available when you select **Auto Computed T_J** and **Estimated Theta J_A**. ■ If you select **None (Conservative)**, the thermal model assumes no heat is dissipated through the board. This results in a pessimistic calculated junction temperature. ■ If you select **JEDEC (2s2p)**, the thermal model assumes the characteristics of the JEDEC 2s2p test board specified in standard JESD51-9. ■ If you select **Typical Board**, the thermal model assumes the characteristics of a typical customer board stack, which is based on selected device and package. You need to perform a detailed thermal simulation of your system to determine the final junction temperature. This two-resistor thermal model is for early estimation only.

Figure 3–1 shows the **Main** section of the PowerPlay Early Power Estimator.

Figure 3–1. PowerPlay Early Power Estimator Spreadsheet Main Section



Logic

A design is a combination of several design modules operating at different frequencies and toggle rates. Each design module can have a different amount of logic. For the most accurate power estimation, partition the design into different design modules. You can partition your design by grouping modules by clock frequency, location, hierarchy, or entities.

Each row in the **Logic** section represents a separate design module. You must enter the following parameters for each design module:

- Clock frequency (f_{MAX}) in MHz
- Number of combinational adaptive look-up tables (ALUTs)
- Number of registers
- Toggle percentage
- Average fanout

Table 3–2 describes the values that need to be entered in the Logic section of the PowerPlay Early Power Estimator.

Table 3–2. Logic Section Information (Sheet 1 of 2)

Input Parameter	Description
Module	Enter a name for each module of the design.
# Combinational ALUTs	Enter the number of combinational ALUTs. For Arria II GX devices, this is the “Combinational ALUTs" value from the Quartus II Compilation Report Resource Usage Summary section. Each Arria II GX adaptive logic module (ALM) contains up to two combinational ALUTs. Smaller ALUTs consume less power than larger ALUTs, but the device can fit more of them. The total number of ALUTs in the design should not exceed (number of ALMs) × two.
# FF	Enter the number of flipflops (FFs) in the module. For Arria II GX devices, this is the sum of "Register ALUTs" and "Dedicated logic registers" from the Quartus II Compilation Report Resource Usage Summary section. Clock routing power is calculated separately on the **Clocks** section of the PowerPlay Early Power Estimator.
Clock Freq (MHz)	Enter a clock frequency (in MHz). This value is limited by the maximum frequency specification for the device family. 100 MHz with a 12.5% toggle means that each LUT or flipflop output toggles 12.5 million times per second (100 × 12.5%).
Toggle %	Enter the average percentage of logic toggling on each clock cycle. The toggle percentage ranges from 0 to 100%. Typically, the toggle percentage is 12.5%, which is the toggle percentage of a 16-bit counter. To ensure you do not underestimate the toggle percentage, you can use a higher toggle percentage. Most logic only toggles infrequently, and hence toggle rates of less than 50% are more realistic. For example, a T-flipflop (TFF) with its input tied to V_{CC} has a toggle rate of 100% because its output is changing logic states on every clock cycle (Table 3–2). Figure 3–3 shows an example of a 4-bit counter. The first TFF with the least significant bit output `cout0` has a toggle rate of 100% because the signal toggles on every clock cycle. The toggle rate for the second TFF with output `cout1` is 50% because the signal only toggles on every two clock cycles. Consequently, the toggle rate for the third TFF with output `cout2` and fourth TFF with output `cout3` are 25% and 12.5%, respectively. Therefore, the average toggle percentage for this 4-bit counter is (100 + 50 + 25 + 12.5) / 4 = 46.875%.
Average Fanout	Enter the average number of blocks fed by the outputs of the LUTs and FFs.
Routing	This shows the power dissipation due to estimated routing (in W). Routing power is highly dependent on placement and routing, which is itself a function of design complexity. The values shown are representative of routing power based on experimentation on over 100 designs. Use the Quartus II PowerPlay Power Analyzer for detailed analysis based on the routing used in your design.
Block	This shows the power dissipation due to internal toggling of the ALMs (in W). Logic block power is a combination of the function implemented and relative toggle rates of the various inputs. The PowerPlay Early Power Estimator spreadsheet uses an estimate based on observed behavior across over 100 real-world designs. Use the Quartus II PowerPlay Power Analyzer for accurate analysis based on the exact synthesis of your design.

Table 3–2. Logic Section Information (Sheet 2 of 2)

Input Parameter	Description
Total	This shows the total power dissipation (in W). The total power dissipation is the sum of the routing and block power.
User Comment	Enter any comments. This is an optional entry.

Figure 3–2. TFF Example

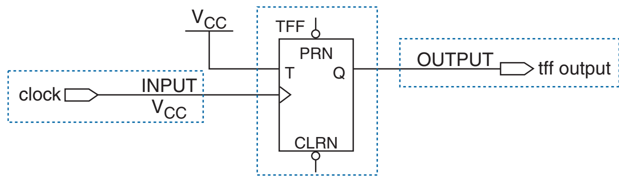


Figure 3–3. 4-Bit Counter Example

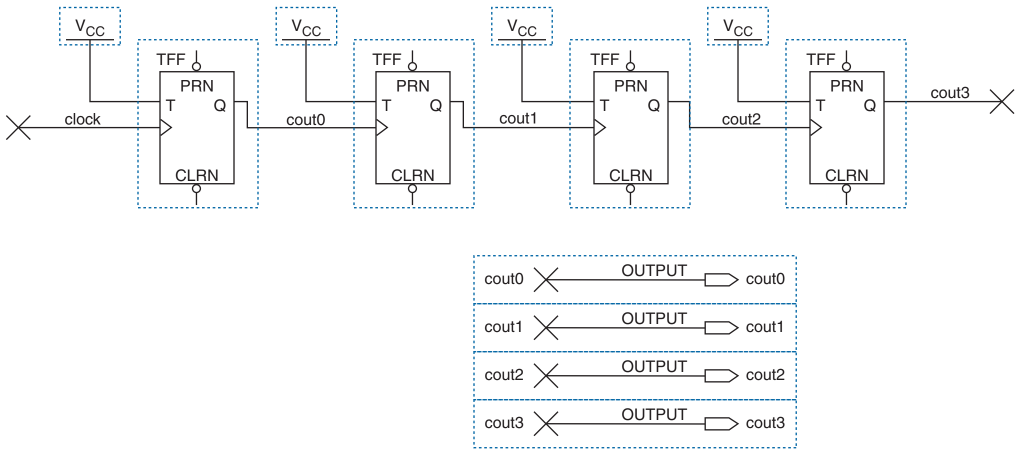


Figure 3–4 shows the device PowerPlay Early Power Estimator spreadsheet and the estimated power consumed by the logic in this design example.

Figure 3–4. Logic Section in the PowerPlay Early Power Estimator

Logic	Return To Main
Total Thermal Power (W)	0.299
Estimated LUT Utilization	88.4%
FF Utilization	96.7%

Module	# Combinational ALUTs	# FFs	Clock Freq (MHz)	Toggle %	Average Fanout	Thermal Power (W) Routing	Block	Total
1	23	20	50	12.5%	3	0.000	0.000	0.000
2	10	100	500	12.5%	3	0.002	0.001	0.002
3	500	400	123	12.5%	3	0.003	0.002	0.005
4	10	2620	250	12.5%	3	0.019	0.008	0.027
5	79	800	334	12.5%	3	0.008	0.004	0.012
6	95	1000	88.4	12.5%	3	0.003	0.001	0.004
7	900	2604	237.8	12.5%	3	0.022	0.013	0.035
8	1265	782	79.9	12.5%	3	0.004	0.003	0.007
9	7940	1580	372	12.5%	3	0.070	0.085	0.155
10	457	2430	438	12.5%	3	0.034	0.018	0.052

RAM Blocks

Arria II GX devices consist of two types of RAM blocks: MLAB and M9K. The power consumption for each type of RAM block is different and must be specified in the **RAM** section of the PowerPlay Early Power Estimator.

Each row in the **RAM** section represents a design module where the RAM block(s) are the same type, have the same data width, the same RAM depth (if applicable), the same RAM mode, and the same port parameters. If some or all of the RAM blocks in your design have different configurations, enter the information in different rows. For each design module, you need to enter the type of RAM being implemented, the number of RAM blocks, and the RAM block mode. Each row on the Early Power Estimator's RAM page represents a logical RAM module which may be physically implemented on more than one RAM block. The Early Power Estimator will always implement each logical RAM module with the minimum number of physical RAM blocks, and in the most power efficient way possible, based on the width and depth of the logical instance entered.

You must also enter the following parameters for each port:

- Clock frequency (in MHz)
- The percentage of time the RAM clock is enabled
- The percentage of time the port is writing compared to reading

When selecting RAM block mode, you must know how your RAM is implemented by the Quartus II Compiler. For example, if a ROM is implemented with two ports, it is considered a true dual-port memory and not a ROM. Single-port and ROM implementations only use Port A. Simple dual-port and true dual-port implementations use Port A and Port B.

Table 3–3 describes the parameters in the **RAM** section of the PowerPlay Early Power Estimator.

Table 3–3. RAM Section Information (Sheet 1 of 3)

Input Parameter	Description
Module	Enter a name for the RAM module in this column. This is an optional value.
RAM Type	Select whether the RAM is implemented as an MLAB or M9K block. The RAM type can be found in the Type column of the Quartus II Compilation Report. In the **Compilation Report**, select **Fitter**, and click **Resource Section**. Click **RAM Summary**.
# RAM Blocks	Enter the number of RAM blocks in the module that use the same type and mode and have the same parameters for each port. The parameters for each port are: ■ clock frequency in MHz ■ percentage of time the RAM is enabled ■ percentage of time the port is writing as opposed to reading The number of RAM blocks can be found in either the MLAB or M9K column of the Quartus II Compilation Report. In the **Compilation Report**, select **Fitter**, and click **Resource Section**. Click **RAM** Summary.
RAM Depth	Enter the depth of the RAM block. The depth of the RAM block can be found in the Port A Depth or the Port B Depth column of the Quartus II Compilation Report. In the **Compilation Report**, select **Fitter**, and click **Resource Section**. Click **RAM** Summary.
Data Width	Enter the width of the data for the RAM block. This value is limited based on the RAM type. The width of the RAM block can be found in the Port A Width or the Port B Width column of the Quartus II Compilation Report. In the **Compilation Report**, select **Fitter**, and click **Resource Section**. Click **RAM** Summary. For RAM blocks that have different widths for Port A and Port B, use the larger of the two widths. This number must be an integer. The valid range for each RAM type is: ■ 1-10 for MLAB using x64 RAM depth ■ 1-20 for MLAB using x32 RAM depth ■ 1-36 (1-18 for True Dual-Port) for M9K
RAM Mode	Select from the following modes: ■ **Single-Port** ■ **Simple Dual-Port** ■ **True Dual-Port** ■ **ROM** The mode is based on how the Quartus II Compiler implements the RAM. If you are unsure how your memory module is implemented, Altera recommends compiling a test case in the required configuration in the Quartus II software. The RAM mode can be found in the Mode column of the Quartus II Compilation Report. In the **Compilation Report**, select **Fitter**, and click **Resource Section**. Click **RAM** Summary. A single-port RAM has one port with a R/W control signal. A simple dual-port RAM has one read port and one write port. A true dual-port RAM has two ports, each with a R/W control signal. ROMs are read-only single-port RAMs.
Port A — Clock Freq	Enter the clock frequency for Port A of the RAM block(s) in MHz. This value is limited by the maximum frequency specification for the RAM type and device family.

Table 3–3. RAM Section Information (Sheet 2 of 3)

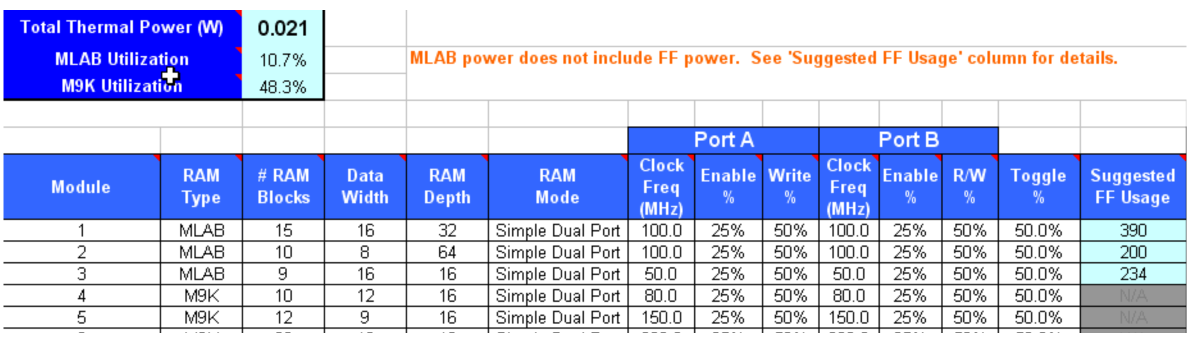
Input Parameter	Description
Port A – Enable %	Enter the average percentage of time the input clock enable for Port A is active, regardless of activity on RAM data and address inputs. The enable percentage ranges from 0 to 100%. The default is set to 25%. RAM power is primarily consumed when a clock event occurs. Using a clock enable signal to disable a port when no read or write operation is occurring can result in significant power savings.
Port A – Write %	Enter the average percentage of time Port A of the RAM block is in write mode versus read mode. For simple dual-port (1R/1W) RAMs, the write port (A) is inactive when not executing a write. For single-port and true dual-port RAMs, port A reads when not written to. This field is ignored for RAMs in ROM mode. This value must be a percentage number between 0% and 100%. The default is 50%.
Port B – Clock Freq	Enter the clock frequency for Port B of the RAM block(s) in MHz. This value is limited by the maximum frequency specification for the RAM type and device family. Port B is ignored for RAM blocks in ROM or single-port mode or when the chosen RAM type is MLAB.
Port B – Enable %	Enter the average percentage of time the input clock enable for Port B is active, regardless of activity on RAM data and address inputs. The enable percentage ranges from 0 to 100%. The default is set to 25%. Port B is ignored for RAM blocks in ROM or single-port mode or when the chosen RAM type is MLAB. RAM power is primarily consumed when a clock event occurs. Using a clock enable signal to disable a port when no read or write operation is occurring can result in significant power savings.
Port B – R/W %	For RAM blocks in true dual-port mode, enter the average percentage of time Port B of the RAM block is in write mode versus read mode. For RAM blocks in simple dual-port mode, enter the percentage of time Port B of the RAM block is reading. You cannot write to Port B in simple dual-port mode. Port B is ignored for RAM blocks in ROM or single-port mode or when the chosen RAM type is MLAB. This value must be a percentage number between 0% and 100%. The default is 50%.
Toggle %	The average percentage for how often each block output signal changes value on each enabled clock cycle is multiplied by the clock frequency and enable percentage to determine the number of transitions per second. This only affects routing power. 50% corresponds to a randomly changing signal. A random signal changes states only half the time.
Suggested FF Usage	Displays the number of FFs needed to make the MLAB function correctly. The MLAB power in the **RAM** section does not include the power of the FFs. If you are manually entering the device resources, add the suggested number of FFs to the **Logic** section using the same clock frequency. No action is required if the device resources have been imported from the PowerPlay Early Power Estimator file. This field is only valid when the chosen RAM type is MLAB.
Valid Width/Mode	This check fails if the entered data width or RAM mode is not compatible with the selected RAM type. See the description of the data width column for the range of available widths for each RAM type.

Table 3–3. RAM Section Information (Sheet 3 of 3)

Input Parameter	Description
Routing	This shows the power dissipation due to estimated routing (in W). Routing power is highly dependent on placement and routing, which is itself a function of design complexity. The values shown are representative of routing power based on experimentation on over 100 customer designs. Use the Quartus II PowerPlay Power Analyzer for detailed analysis based on the routing used in your design. This value is calculated automatically.
Block	This shows the power dissipation due to internal toggling of the RAM (in W). Use the Quartus II PowerPlay Power Analyzer for accurate analysis based on the exact RAM modes in your design. This value is calculated automatically.
Total	This shows the estimated power in W, based on the inputs you entered. It is the total power consumed by RAM blocks and is equal to the routing power and the block power. This value is calculated automatically.
User Comment	Enter any comments. This is an optional entry.

Figure 3–5 shows the PowerPlay Early Power Estimator spreadsheet and the estimated power consumed by RAM blocks in this design.

Figure 3–5. RAM Section in the PowerPlay Early Power Estimator



Total Thermal Power (W)	0.021
MLAB Utilization	10.7%
M9K Utilization	48.3%

MLAB power does not include FF power. See 'Suggested FF Usage' column for details.

						Port A			Port B				
Module	RAM Type	# RAM Blocks	Data Width	RAM Depth	RAM Mode	Clock Freq (MHz)	Enable %	Write %	Clock Freq (MHz)	Enable %	R/W %	Toggle %	Suggested FF Usage
1	MLAB	15	16	32	Simple Dual Port	100.0	25%	50%	100.0	25%	50%	50.0%	390
2	MLAB	10	8	64	Simple Dual Port	100.0	25%	50%	100.0	25%	50%	50.0%	200
3	MLAB	9	16	16	Simple Dual Port	50.0	25%	50%	50.0	25%	50%	50.0%	234
4	M9K	10	12	16	Simple Dual Port	80.0	25%	50%	80.0	25%	50%	50.0%	N/A
5	M9K	12	9	16	Simple Dual Port	150.0	25%	50%	150.0	25%	50%	50.0%	N/A

Digital Signal Processing (DSP)

Arria II GX devices have dedicated DSP blocks that can implement high-speed parallel processing optimized for DSP applications. DSP blocks are ideal for implementing DSP applications that need high data throughput. The **Digital Signal Processing (DSP)** section in the PowerPlay Early Power Estimator spreadsheet provides power information for Arria II GX DSP blocks.

Each row in the **DSP** section represents a DSP design module where all instances of the module have the same configuration, clock frequency, toggle percentage, and register usage. If some (or all) DSP or multiplier instances have different configurations, you need to enter the information in different rows. You must enter the following information for each DSP or multiplier module:

- Configuration
- Number of instances
- Clock frequency (f_{MAX}) in MHz
- Toggle percentage of the data outputs

- Whether or not the inputs and outputs are registered
- Whether or not the module is pipelined

For more information about Arria II GX DSP block configurations, refer to the *DSP Blocks in Arria II GX Devices* chapter in volume 1 of the *Arria II GX Device Handbook*.

Table 3–4 describes the values that need to be entered in the **DSP** section of the PowerPlay Early Power Estimator.

Table 3–4. DSP and Multiplier Section Information

Input Parameter	Description
Module	Enter a name for the DSP module in this column. This is an optional value.
Configuration	Select the DSP block configuration for the module.
# of Instances	Enter the number of DSP block instances that have the same configuration, clock frequency, toggle percentage, and register usage. This value is independent of the number of dedicated DSP blocks being used. For example, it is possible to use four 9 × 9 simple multipliers that would all be implemented in the same DSP block in Arria II GX devices. In this case, the number of instances would be four.
Clock Freq (MHz)	Enter the clock frequency for the module in MHz. This value is limited by the maximum frequency specification for the device family.
Toggle %	Enter the average percentage of DSP data outputs toggling on each clock cycle. The toggle percentage ranges from 0 to 50%. Typically the toggle percentage is 12.5%. For a more conservative power estimate, you can use a higher toggle percentage. In addition, 50% corresponds to a randomly changing signal (since half the time the signal changes from a 0 –> 0 or 1 –> 1). This is considered the highest meaningful toggle rate for a DSP block.
Reg Inputs?	Select whether the inputs to the dedicated DSP block or multiplier block are registered using the dedicated input registers. If the dedicated input registers in the DSP or multiplier block are being used, select **Yes**. If the inputs are unregistered or registered using registers in ALMs, select **No**.
Reg Outputs?	Select whether the outputs of the dedicated DSP block or multiplier block are registered using the dedicated output registers. If the dedicated output registers in the DSP or multiplier block are being used, select **Yes**. If the outputs are unregistered or registered using registers in ALMs, select **No**.
Pipe-lined?	Select whether the dedicated DSP block is pipelined.
Routing	This shows the power dissipation due to estimated routing (in W). Routing power is highly dependent on placement and routing, which is itself a function of design complexity. The values shown are representative of routing power based on experimentation on over 100 customer designs. Use the Quartus II PowerPlay Power Analyzer for detailed analysis based on the routing used in your design. This value is calculated automatically.
Block	This shows the estimated power consumed by the DSP blocks (in W). This value is calculated automatically.
Total	This shows the estimated power (in W), based on the inputs you entered. It is the total power consumed by DSP blocks and is equal to the routing power and the block power. This value is calculated automatically.
User Comment	Enter any comments. This is an optional entry.

Figure 3–6 shows the PowerPlay Early Power Estimator spreadsheet and the estimated power consumed by the DSP blocks.

Figure 3–6. DSP Section in the PowerPlay Early Power Estimator

DSP | Return to Main

Total Thermal Power (W)	0.018
DSP Utilization	97.6%

Module	Configuration	# of Instances	Clock Freq (MHz)	Toggle %	Reg Inputs?	Reg Outputs?	Pipe-lined?	Thermal Power (W) Routing	Block	Total
1	9x9 Simple Mult	8	222.0	12.5%	Yes	Yes	Yes	0.001	0.002	0.003
2	12x12 Simple Mult	5	154.0	12.5%	Yes	Yes	Yes	0.001	0.001	0.002
3	18x18 Simple Mult	6	50.0	12.5%	Yes	Yes	Yes	0.000	0.001	0.001
4	36x36 Simple Mult	4	200.0	12.5%	Yes	Yes	Yes	0.002	0.007	0.008
5	18x18 Two-Mult Adder	4	123.0	12.5%	Yes	Yes	Yes	0.000	0.002	0.002
6	18x18 Two-Mult Adder with Loopback	2	66.0	12.5%	Yes	Yes	Yes	0.000	0.001	0.001

General I/O Pins

Arria II GX devices feature programmable I/O pins that support a wide range of industry I/O standards for increased design flexibility. The I/O section in the PowerPlay Early Power Estimator spreadsheet allows you to estimate the I/O pin power consumption based on the I/O standard of the pin.

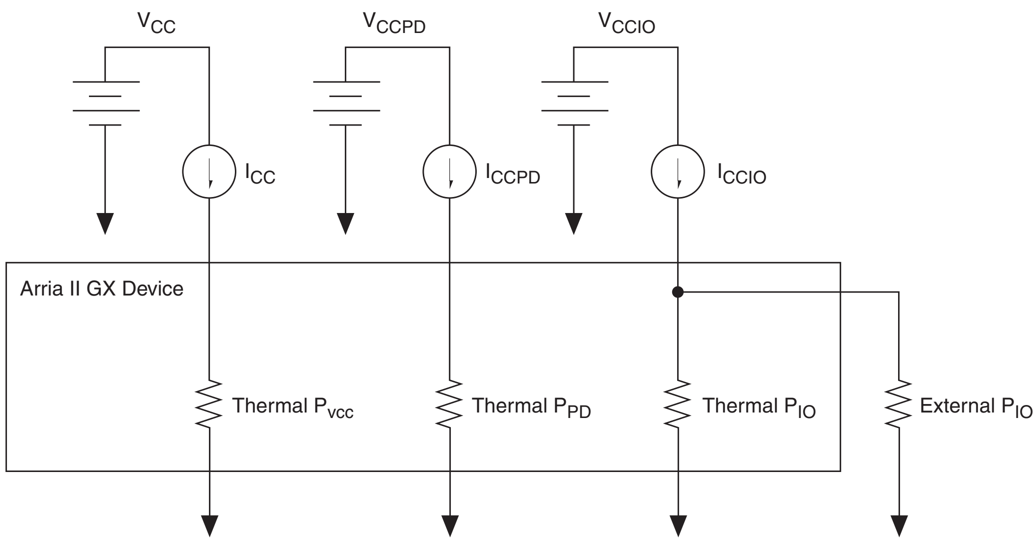
The PowerPlay Early Power Estimator spreadsheet assumes you are using external termination resistors when you design with I/O standards that recommend termination resistors (SSTL and HSTL). If your design does not use external termination resistors, you need to choose the LVTTL/LVCMOS I/O standard with the same V_{CCIO} and similar current strength as the terminated I/O standard. For example, if you are using the SSTL-2 Class II I/O standard without termination resistors (using a point-to-point connection), you need to select 2.5 V as your I/O standard and 16 mA as the current strength in the PowerPlay Early Power Estimator.

The power reported for I/O signals includes thermal and external I/O power. The total thermal power is the sum of the thermal power consumed by the device from each power rail.

thermal power = thermal P_{VCC} + thermal P_{PD} + thermal P_{IO}

Figure 3–7 shows a graphical representation of I/O power consumption. The I_{CCIO} rail power includes both the thermal P_{IO} and the external P_{IO}.

Figure 3–7. I/O Power Representation



The V_{REF} pins consume minimal current (less than 10 mA) and is negligible when compared to the power consumed by the general purpose I/O pins. Therefore, the PowerPlay Early Power Estimator spreadsheet does not include the current for V_{REF} pins in the calculations.

Each row in the I/O section represents a design module where the I/O pins have the same I/O standard, input termination, current strength or output termination, data rate, clock frequency, output enable static probability, and capacitive load. You must enter the following parameters for each design module:

- I/O standard
- Input Termination
- Current strength/Output termination
- Slew rate
- Number of input, output, and bidirectional pins
- I/O data rate
- Clock frequency (f_{MAX}) in MHz
- Average pin toggle percentage
- Output enable static probability
- Capacitance of the load

Table 3–5 describes the I/O power rail information in the **I/O** section of the PowerPlay Early Power Estimator.

Table 3–5. I/O Power Rail Information in the I/O Section

Input Parameter	Description
Power Rails	Power supply rails for the I/O pins.
Voltage (V)	The voltage applied to the specified power rails in Volts (V).
Current (A)	The current drawn from the specified power rails in Amps (A).

Table 3–6 describes the I/O module parameters in the **I/O** section of the PowerPlay Early Power Estimator.

Table 3–6. I/O Module Information in the I/O Section (Sheet 1 of 2)

Input Parameter	Description
Module	Enter a name for the module in this column. This is an optinal value.
I/O Standard	Select the I/O standard used for the input, output, or bidirectional pins in this module from the list. The calculated I/O power varies based on the I/O standard. For I/O standards that recommend termination (SSTL and HSTL), the PowerPlay Early Power Estimator spreadsheet assumes you are using external termination resistors. If you are not using external termination resistors, you need to choose the LVTTL/LVCMOS I/O standard with the same voltage and current strength as the terminated I/O standard. There are up and down scroll bars to view all the I/O standards in the drop-down list.
Input Termination	Select the input termination setting implemented for the input and bidirectional pin(s) in this module.
Current Strength/ Output Termination	Select the current strength or output termination implemented for the output and bidirectional pin(s) in this module. Current strength and output termination are mutually exclusive.
Slew Rate	Select the slew rate setting for the output and bidirectional pin(s) in this module. Using a lower slew rate setting helps reduce switching noise but may increase delay.
# Input Pins	Enter the number of input pins used in this module. A differential pair of pins should be considered as one pin.
# Output Pins	Enter the number of output pins used in this module. A differential pair of pins should be considered as one pin.
# Bidir Pins	Enter the number of bidirectional pins used in this module. The I/O pin is treated as an output when its output enable signal is active and an input when the output enable is disabled. An I/O configured as bidirectional but used only as an output consumes more power than one configured as an output-only, due to the toggling of the input buffer every time the output buffer toggles (they share a common pin).
Data Rate	Select either **SDR** or **DDR** as the I/O data rate. This indicates whether the I/O value is updated once (SDR) or twice (DDR) a cycle. If the data rate of the pin is DDR, it is possible to set the data rate to SDR and double the toggle percentage. The Quartus II software often uses this method to output information.
Clock Freq (MHz)	Enter the clock frequency (in MHz). This value is limited by the maximum frequency specification for the device family. 100 MHz with a 12.5% toggle means that each I/O pin toggles 12.5 million times per second (100 × 12.5%).

Table 3–6. I/O Module Information in the I/O Section (Sheet 2 of 2)

Input Parameter	Description
Toggle %	Enter the average percentage of input, output, and bidirectional pins toggling on each clock cycle. The toggle percentage ranges from 0 to 200% for input pins used as clocks because clocks toggle at twice the frequency. If the pins use DDR circuitry, you can set the data rate to SDR and double the toggle percentage. The Quartus II software often uses this method to output information. Typically the toggle percentage is 12.5%. To be more conservative, you can use a higher toggle percentage.
OE %	Enter the average percentage of time that: ■ Output I/O pins are enabled. ■ Bidirectional I/O pins are outputs and enabled. During the remaining time: ■ Output I/O pins are tristated. ■ Bidirectional I/O pins are inputs. This number must be a percentage between 0% and 100%.
Load (pF)	Enter the pin loading external to the chip (in pF). This only applies to outputs and bidirectional pins. Pin and package capacitance is already included in the I/O model. Therefore, you only need to include off-chip capacitance in the Load parameter.
Thermal Power (W), Routing	This shows the power dissipation due to estimated routing (in W). Routing power is highly dependent on placement and routing, which is itself a function of design complexity. The values shown are representative of routing power based on experimentation on over 100 customer designs. Use the Quartus II PowerPlay Power Analyzer for detailed analysis based on the routing used in your design. This value is calculated automatically.
Thermal Power (W), Block	This shows the power dissipation due to internal and load toggling of the I/O (in W). Use the Quartus II PowerPlay Power Analyzer for accurate analysis based on the exact I/O configuration of your design. This value is calculated automatically.
Thermal Power (W), Total	This shows the total power dissipation (in W). The total power dissipation is the sum of the routing and block power. This value is calculated automatically.
Supply Current (A), I_{CC}	This shows the current drawn from the V_{CC} rail. Powers internal digital circuitry. This value is calculated automatically.
Supply Current (A), I_{CCPD}	This shows the current drawn from the V_{CCPD} rail. This rail powers the pre-drive circuitry. This value is calculated automatically.
Supply Current (A), I_{CCIO}	This shows the current drawn from the V_{CCIO} rail. Some of this current may be drawn into off-chip termination resistors. This value is calculated automatically.
User Comments	Enter any comments. This is an optional entry.

Figure 3–8 shows the I/O module parameters in the PowerPlay Early Power Estimator spreadsheet I/O section.

For more information about Arria II GX I/O standard termination scheme, refer to the *Arria II GX Device I/O Features* chapter in volume 1 of the *Arria II GX Device Handbook*.

Figure 3–8. PowerPlay Early Power Estimator Spreadsheet I/O Section

I/O	Return To Main
Total Thermal Power (W)	0.782
I/O Utilization	77.9%

Power Rails	Voltage (V)	Current (A)
V_{CCIO}	1.2	0.0007
V_{CCIO}	1.5	0.0446
V_{CCIO}	1.8	0.7878
V_{CCIO}	2.5	0.0723
V_{CCIO}	3.0	0.0015
V_{CCIO}	3.3	0.0021
V_{CCPD}	2.5	0.0330
V_{CCPD}	3.0	0.0008
V_{CCPD}	3.3	0.0018

Differential I/O standards are being used. Please check that each differential pin pair is entered as one pin.

												Thermal Power (W)			Supply Current (A)		
Module	I/O Standard	Input Termination	Current Strength / Output Termination	Slew Rate	# Input Pins	# Output Pins	# Bidir Pins	Data Rate	Clock Freq (MHz)	Toggle %	OE %	Load (pF)	Routing	Block	Total	I_{CC}	I_{CCPD}	I_{CCIO}
1	2.5 V	Off	4mA	1	0	20	0	SDR	50.0	12.5%	100.0%	5	0.000	0.006	0.006	0.000	0.001	0.002
2	1.2 V	Off	4mA	1	0	0	10	SDR	75.0	12.5%	100.0%	5	0.000	0.003	0.003	0.001	0.001	0.001
3	3.3-V LVCMOS	Off	2mA	1	50	0	0	SDR	200.0	12.5%	100.0%	5	0.001	0.011	0.012	0.003	0.001	0.002
4	3.0-V PCI	Off	Default	1	0	6	0	SDR	100.0	12.5%	100.0%	5	0.000	0.007	0.007	0.000	0.001	0.001
5	1.8-V HSTL Class II	Off	16mA	1	0	64	0	SDR	66.0	12.5%	100.0%	5	0.000	0.468	0.468	0.002	0.004	0.788
6	1.5-V HSTL Class I	Off	8mA	1	0	0	10	SDR	150.0	12.5%	100.0%	5	0.000	0.087	0.087	0.003	0.022	0.045
7	LVDS	Differential	Default	N/A	0	16	0	SDR	100.0	12.5%	100.0%	5	0.000	0.155	0.155	0.020	0.000	0.062
8	2.5 V	Off	4mA	1	0	0	20	SDR	250.0	12.5%	100.0%	5	0.001	0.030	0.031	0.002	0.003	0.009

High-Speed Differential Interface (HSDI)

Arria II GX devices feature dedicated circuitry that interface with high-speed differential I/O standards. These are dedicated transmitters and receivers that contain serializer and deserializer blocks, respectively. The **high-speed differential interface (HSDI)** section in the PowerPlay Early Power Estimator spreadsheet is divided into receiver and transmitter parts.

The power calculated in the **HSDI** section only applies to the transmitter serializer block or the receiver deserializer block. The transmitter and receiver are implemented using the ALTLVDS megafunction. The I/O buffer power is calculated in the I/O section and the PLL power is calculated in the **PLL** section.

Each row in the **HSDI** section represents a separate receiver or transmitter domain. You must enter the following parameters for transmitter and receiver domains:

- Data rate (in Mbps)
- Number of channels in that transmitter domain
- Toggle percentage

The receiver power is the same whether or not you use the DPA circuitry.

Table 3–7 describes the parameters in the HSDI section of the PowerPlay Early Power Estimator.

Table 3–7. HSDI Section Information

Input Parameter	Description
TX/RX Module	Enter a name for the module in this column. This is an optional value.
Data Rate (Mbps)	Enter the maximum data rate in Mbps of the receiver or transmitter module. The serializer/deserializer (SERDES) circuitry can transmit and receive data up to 1,250 Mbps per channel. Therefore, the data rate must be a decimal number from 0 to 1,250 Mbps.
# of Channels	Enter the number of receiver and transmitter channels running at the data rate shown in “Data Rate (Mbps)”. This number must be an integer value from 0 to 156.
Toggle %	Enter the average percentage of toggling on each clock cycle. The toggle % ranges from 0 to 100%. The default toggle percentage is 50%.
Serialization Factor/ Deserialization Factor	Enter the number of parallel data bits for each serial data bit. This number must be an integer value from 1 to 10.
Total Power	This shows the estimated power (in W), based on the data rate and number of channels entered. This value is calculated automatically.
User Comments	Enter any comments. This is an optional entry.

Figure 3–9 shows the PowerPlay Early Power Estimator spreadsheet and the estimated power consumed by HSDI blocks for this design.

Figure 3–9. HSDI Section in the PowerPlay Early Power Estimator

HSDI	Return to Main
Total Thermal Power (W)	0.008
Tx Channel Utilization	83.3%
Rx Channel Utilization	83.3%

This section only estimates power within the SERDES blocks and does not include the I/O power nor PLL power.
Please enter the appropriate parameters in the "IO" section for I/O power, and "PLL" section for PLL power.

Tx Module	Data Rate (Mbps)	# of Channels	Serialization Factor	Toggle %	Total Power (W)	User Comments
1	266	8	7	50.0%	0.001	
2	300	12	7	50.0%	0.002	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	

Rx Module	Data Rate (Mbps)	# of Channels	Deserialization Factor	Toggle %	Total Power (W)	User Comments
1	266	8	7	50.0%	0.002	
2	300	12	7	50.0%	0.003	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	

Phase-Locked Loops (PLLs)

Arria II GX devices feature top/bottom and left/right PLLs for general usage. If you are using dedicated transmitters or receivers and are using an LVDS PLL to implement serialization or deserialization, specify an LVDS PLL and enter power information in the **PLL** section.

When a left/right PLL drives LVDS hardware, it is referred to as an LVDS PLL. LVDS PLLs drive LVDS clock trees and DPA buses at the VCO frequency (600 to 1300 MHz). If an LVDS PLL drives LVDS hardware only, enter the appropriate VCO frequency and specify an output frequency of 0 MHz. If the LVDS PLL also drives a clock to a pin or to the core, specify that clock frequency as the output frequency (0 to 720 MHz).

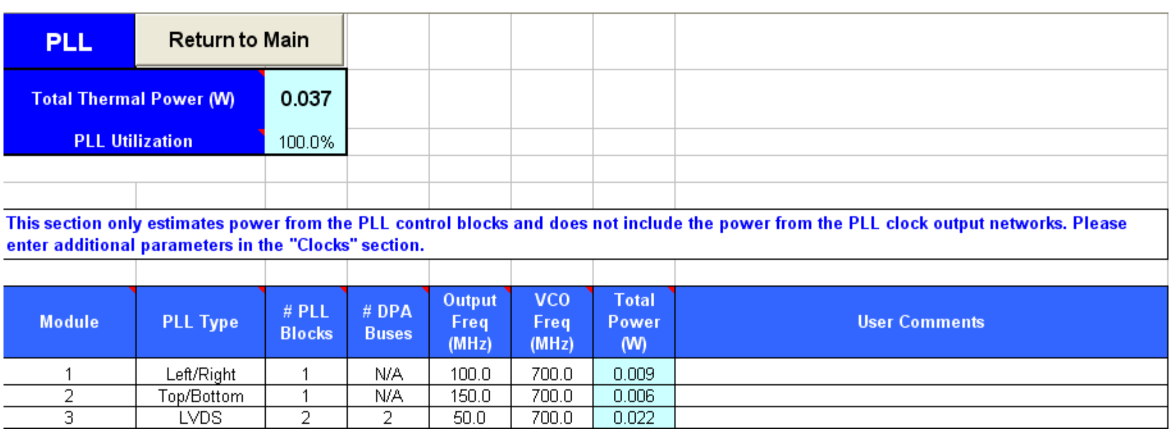
Each row in the **PLL** section represents one or more PLLs in the device. You need to enter the maximum output frequency and the VCO frequency for each PLL. You must also specify whether each PLL is an LVDS, left/right, or top/bottom PLL. Table 3–8 describes the values that need to be entered in the **PLL** section of the PowerPlay Early Power Estimator.

Table 3–8. PLL Section Information

Input Parameter	Description
Module	Enter a name for the PLL in this column. This is an optional value.
PLL Type	Select whether the PLL is an LVDS, left/right, or top/bottom PLL.
# PLL Blocks	Enter the number of PLL blocks with the same specific output frequency and VCO frequency combination.
# DPA Buses	Enter the number of dynamic phase alignment (DPA) buses in use. DPA is only available for LVDS PLLs.
Output Freq (MHz)	Enter the maximum output frequency (f_{MAX}) of the PLL (in MHz). The maximum output frequency is reported in the Output Frequency column of the Quartus II Compilation Report. In the **Compilation Report**, select **Fitter**, and click **Resource Section**. Select **PLL Usage**, and click **Output Frequency**. If there are multiple clock outputs from the PLL, choose the maximum output frequency listed. The output frequency is the same as the VCO frequency for LVDS PLLs used as part of a SERDES.
VCO Freq (MHz)	Enter the frequency of the voltage controlled oscillator in MHz. The VCO frequency is reported in the Nominal VCO frequency row of the Quartus II Compilation Report. In the **Compilation Report**, select **Fitter**, and click **Resource Section**. Select **PLL Summary**, and click **Nominal VCO frequency**.
Total Power (W)	Total Power (W) shows the estimated combined power for VCCA and VCCD (in W), based on the maximum output frequency and the VCO frequency you entered. This value is calculated automatically.
User Comments	Enter any comments. This is an optional entry.

Figure 3–10 shows the PowerPlay Early Power Estimator spreadsheet and the estimated power consumed by PLLs in this design.

Figure 3–10. PLL Section in the PowerPlay Early Power Estimator



PLL | Return to Main

Total Thermal Power (W)	0.037
PLL Utilization	100.0%

This section only estimates power from the PLL control blocks and does not include the power from the PLL clock output networks. Please enter additional parameters in the "Clocks" section.

Module	PLL Type	# PLL Blocks	# DPA Buses	Output Freq (MHz)	VCO Freq (MHz)	Total Power (W)	User Comments
1	Left/Right	1	N/A	100.0	700.0	0.009	
2	Top/Bottom	1	N/A	150.0	700.0	0.006	
3	LVDS	2	2	50.0	700.0	0.022	

Clocks

Arria II GX devices have up to a total of 148 clock domains available that can be on either a global or regional clock network. There are 16 global clocks and up to 48 regional clocks per quadrant for a total of 88 regional clocks. The PowerPlay Early Power Estimator spreadsheet does not distinguish between global and regional clocks because the difference in power is not significant.

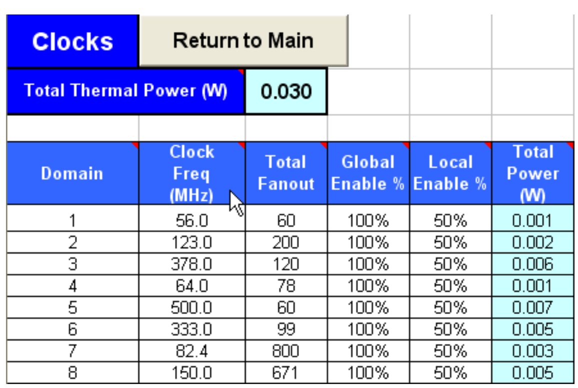
Each row in the **Clocks** section represents a clock network or a separate clock domain. You must enter the clock frequency (f_{MAX}) in MHz, the total fanout for each clock network used, the global clock enable percentage, and the local clock enable percentage. Table 3–10 describes the parameters in the **Clock** section of the PowerPlay Early Power Estimator.

Table 3–9. Clock Section Information

Input Parameter	Description
Domain	Enter a name for the clock network in this column. This is an optional value.
Clock Freq (MHz)	Enter the frequency of the clock domain. This value is limited by the maximum frequency specification for the device family.
Total Fanout	Enter the total number of flipflops and RAM, DSP, and I/O blocks fed by this clock. The number of resources driven by every global clock and regional clock signal is reported in the Fan-out column of the Quartus II Compilation Report. In the **Compilation Report**, select **Fitter** and click **Resource Section**. Select **Global & Other Fast Signals** and click **Fan-out**.
Global Enable %	Enter the average % of time that the entire clock tree is enabled. Each global clock buffer has an enable signal that can be used to dynamically shut down the entire clock tree.
Local Enable %	Enter the average % of time that clock enable is high for destination flipflops. Local clock enables for flipflops in ALMs are promoted to LAB-wide signals. When a given flipflop is disabled, the LAB-wide clock is also disabled, cutting clock power in addition to power for down-stream logic. This sheet models only the impact on clock tree power.
Total Power (W)	This is the total power dissipation due to clock distribution (in W). This value is calculated automatically.
User Comments	Enter any comments. This is an optional entry.

Figure 3–11 shows the PowerPlay Early Power Estimator spreadsheet and the estimated power consumed by clocks for this design.

Figure 3–11. Clocks Section in the PowerPlay Early Power Estimator



Clocks | Return to Main

Total Thermal Power (W) | 0.030

Domain	Clock Freq (MHz)	Total Fanout	Global Enable %	Local Enable %	Total Power (W)
1	56.0	60	100%	50%	0.001
2	123.0	200	100%	50%	0.002
3	378.0	120	100%	50%	0.006
4	64.0	78	100%	50%	0.001
5	500.0	60	100%	50%	0.007
6	333.0	99	100%	50%	0.005
7	82.4	800	100%	50%	0.003
8	150.0	671	100%	50%	0.005

Transceiver (XCVR)

Arria II GX devices feature dedicated embedded circuitry that contain up to 16 high-speed 3.75 Gbps serial transceiver channels. Arria II GX devices have dedicated transmitters and receivers that contain serializer and deserializer blocks, respectively.
.

The power calculated in this section applies to the transceiver blocks, including the channels used and all circuitry used in the clock control unit (CCU). The transceivers are implemented using the ALTGX megafunction. The I/O buffer power and the PLL power for the transceivers are included in this section. Transmitters and receivers assume 100 Ω termination.

The transceivers draw current from four power rails: V_{CCH_GXB}, V_{CCL_GXB}, V_{CC}, and V_{CCA}. Table 3–10 describes the information reported for each rail.

Table 3–10. Transceiver Power Supply Information in the XCVR Section

Column Heading	Description
Power Rails	Power supply rails for the transceiver blocks.
Voltage (V)	The voltage applied to the specified power rail in Volts (V).
Current (A)	The current drawn from the specified power rail in Amps (A).

Each row in the **XCVR** section represents a separate transceiver domain. For each transceiver domain used, you need to enter the number of channels, protocol used, transceiver block operation mode, data rate (in Mbps), width of the parallel data bus, pre-emphasis setting, and VOD setting. For certain modes, you must specify whether the byte serializer, rate match FIFO setting, and 8B/10B encoder features are used.

Table 3–11 describes the values that need to be entered in the **XCVR** section of the PowerPlay Early Power Estimator.

Table 3–11. XCVR Section Information (Sheet 1 of 2)

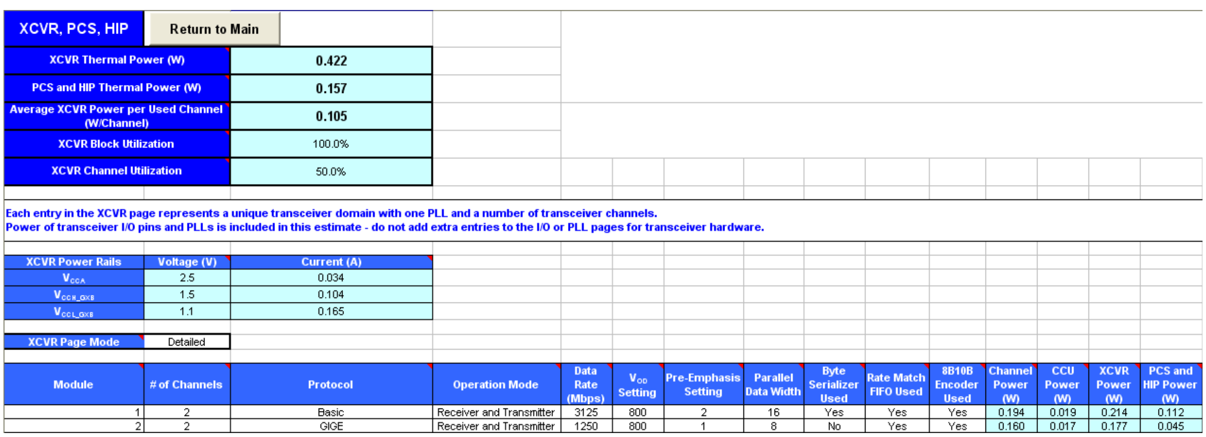
Input Parameter	Description
Module	Enter a name for the module in this column. This is an optional value.
# of Channels Used	Enter the number of channels used in this transceiver domain. These channels are grouped together in one transceiver block or two adjacent transceiver blocks and clocked by a common PLL. The number of channels allowed in each domain depends on selected protocol.
Protocol	Enter the communication protocol or standard these transceivers implement (for example, SONET Backplane OC12, Basic 6G, and so on).
Operation Mode	Enter the operation mode implemented by the transceiver block. Options include: ■ Receiver and Transmitter ■ Receiver only ■ Transmitter only
Data Rate (Mbps)	Enter the data rate the transceivers will operate at (in Mbps).
V_{OD} Setting	Enter the output differential voltage (V_{OD}) setting of the GXB Transmitter channel PMA. It is assumed that the transmitter uses a termination resistance of 100 Ω.
Pre-Emphasis Setting	Enter the pre-emphasis first post-tap setting used by the transmitter.

Table 3–11. XCVR Section Information (Sheet 2 of 2)

Input Parameter	Description
Parallel Data Width	Enter the width of the parallel data bus going into each GXB transmitter channel PCS and coming out of each GXB receiver channel PCS.
Byte Serializer Used	Enter whether or not the byte serializer/deserializer is used. If the byte serializer is used, the transceiver is in double-width mode. If it is not used, the transceiver is in single-width mode.
Rate Match FIFO Used	Enter whether or not the rate matching FIFO is used.
8B/10B Encoder Used	Enter whether or not the 8B/10B encoder/decoder is used.
Channel Power (W)	This shows the total power of the GXB transmitter channel PMA and GXB receiver channel PMA blocks for all channels (in W). This value is calculated automatically.
CCU Power (W)	This shows the total power of the GXB PLLs and control circuitry for all channels (in W). This value is calculated automatically.
XCVR Power (W)	This shows the sum of the channel power and CCU power (in W). This value is calculated automatically.
PCS/HIP Power (W)	This shows the total power of the GXB transmitter channel PCS, GXB receiver channel PCS, and PCI Express hard IP blocks for all channels (in W). This value is calculated automatically.
User Comments	Enter any comments. This is an optional entry.

Figure 3–12 shows the PowerPlay Early Power Estimator spreadsheet and the estimated power comsumed by the XCVR feature for this design.

Figure 3–12. Power Comsumption by the XCVR in the PowerPlay Early Power Estimator



XCVR, PCS, HIP | Return to Main

XCVR Thermal Power (W)	0.422
PCS and HIP Thermal Power (W)	0.157
Average XCVR Power per Used Channel (W/Channel)	0.105
XCVR Block Utilization	100.0%
XCVR Channel Utilization	50.0%

Each entry in the XCVR page represents a unique transceiver domain with one PLL and a number of transceiver channels.
Power of transceiver I/O pins and PLLs is included in this estimate - do not add extra entries to the I/O or PLL pages for transceiver hardware.

XCVR Power Rails	Voltage (V)	Current (A)
V_{CCA}	2.5	0.034
V_{CCH_GXB}	1.5	0.104
V_{CCL_GXB}	1.1	0.165

XCVR Page Mode: Detailed

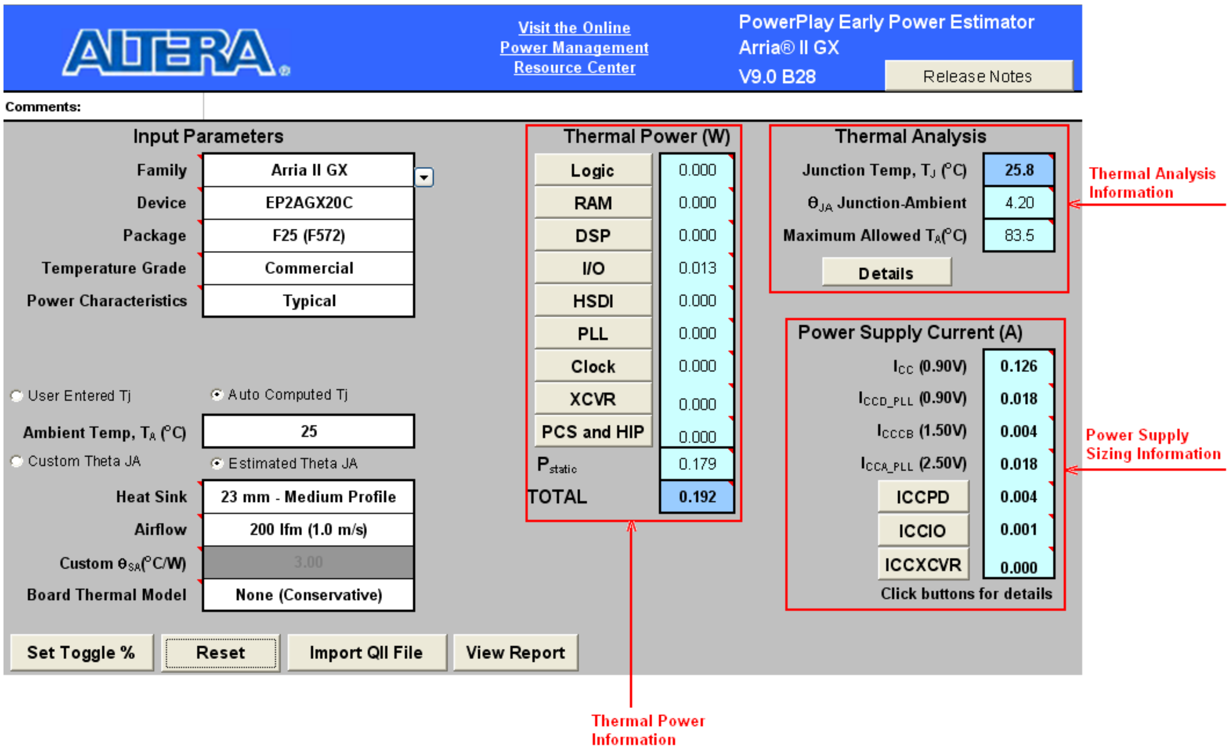
Module	# of Channels	Protocol	Operation Mode	Data Rate (Mbps)	V_{OD} Setting	Pre-Emphasis Setting	Parallel Data Width	Byte Serializer Used	Rate Match FIFO Used	8B10B Encoder Used	Channel Power (W)	CCU Power (W)	XCVR Power (W)	PCS and HIP Power (W)
1	2	Basic	Receiver and Transmitter	3125	800	2	16	Yes	Yes	Yes	0.194	0.019	0.214	0.112
2	2	GIGE	Receiver and Transmitter	1250	800	1	8	No	Yes	Yes	0.160	0.017	0.177	0.045

Power Analysis

The **Main** section of the PowerPlay Early Power Estimator spreadsheet summarizes the power and current estimates for the design. The **Main** section displays the total thermal power, thermal analysis, and power supply sizing information. The accuracy of the information depends on the information entered. The power consumed can also vary greatly depending on the toggle rates entered. The following sections describe of the results provided by the PowerPlay Early Power Estimator.

Figure 3–13 shows the Thermal Power, Thermal Analysis, and Power Supply Sizing areas in the **Main** section.

Figure 3–13. Power Areas in the Main Section



Thermal Power

Thermal power is the power dissipated in the device. The total thermal power is shown in W and is a sum of the thermal power of all the resources used in the device. The total thermal power includes the maximum power from standby and dynamic power.

☞ The total thermal power only includes the thermal component for the **I/O** section and does not include the external power dissipation, such as from voltage-referenced termination resistors.

Figure 3–14 shows the total thermal power in Watts and the static power (P_{STATIC}) consumed by the device. The thermal power for each section is displayed. To see how the thermal power for a section was calculated, click on the section to view the inputs entered for that section.

Figure 3–14. Thermal Power in the PowerPlay Early Power Estimator

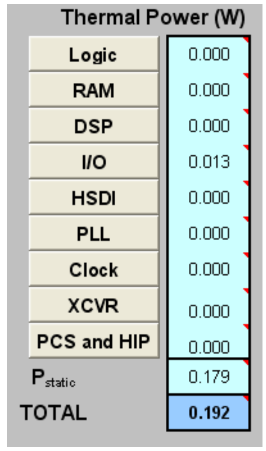


Table 3–12 describes the thermal power parameters in the PowerPlay Early Power Estimator.

Table 3–12. Thermal Power Section Information (Sheet 1 of 2)

Input Parameter	Description
Logic	This shows the dynamic power consumed by ALMs and associated routing. Click **Logic** to see details.
RAM	This shows the dynamic power consumed by RAM blocks and associated routing. Click **RAM** to see details.
DSP	This shows the dynamic power consumed by DSP blocks and associated routing. Click **DSP** to see details.
I/O	This shows the thermal power consumed by I/O pins and associated routing. This includes static power dissipated in terminated I/O standards on chip and stand-by power dissipated in I/O banks. Click **I/O** to see details.
HSDI	This shows the dynamic power consumed by SERDES hardware for high-speed differential I/O. Click **HSDI** to see details.
PLL	This shows the dynamic power consumed by PLLs. Click **PLL** to see details.
Clocks	This shows the dynamic power consumed by clock networks. Click **Clocks** to see details.
XCVR	This shows the thermal power consumed by transceiver hardware. This includes the standby power consumed by unused transceivers. Click the **XCVR** button to see details. If the value equals N/A, transceiver blocks are not available on the chosen device.
PCS and HIP	This shows the thermal power consumed by the GXB transmitter and receiver channel PCS and the PCI Express hard IP (HIP) blocks of the transceiver hardware. This includes the standby power consumed by unused transceivers. Click the **PCS and HIP** button to see details. If the value equals N/A, the transceiver blocks are not available on the chosen device.

Table 3–12. Thermal Power Section Information (Sheet 2 of 2)

Input Parameter	Description
P_{STATIC}	This shows the static power consumed irrespective of clock frequency. This does not include static I/O current due to termination resistors, which is included in the I/O power above. P_{STATIC} is affected by junction temperature, selected device, and power characteristics.
TOTAL	This shows the total power dissipated as heat from the FPGA. This does not include power dissipated in off-chip termination resistors. See "Power Supply Current (A)" on page 3–29 for the current draw from the FPGA supply rails. This may differ due to currents supplied to off-chip components and thus not dissipated as heat in the FPGA.

Thermal Analysis

You can choose to enter $\mathbf{T_J}$ directly or compute $\mathbf{T_J}$ based on information provided. If you choose to enter T_J, select **User Entered $\mathbf{T_j}$** in the **Input Parameters** section. If you choose to automatically compute T_J, select **Auto Computed $\mathbf{T_j}$** in the **Input Parameters** section.

When automatically computing T_J, the device's ambient temperature, airflow, heat sink solution, and board thermal model are considered to determine the junction temperature (T_J) in degrees Celsius. T_J is the estimated operating junction temperature based on your device and thermal conditions.

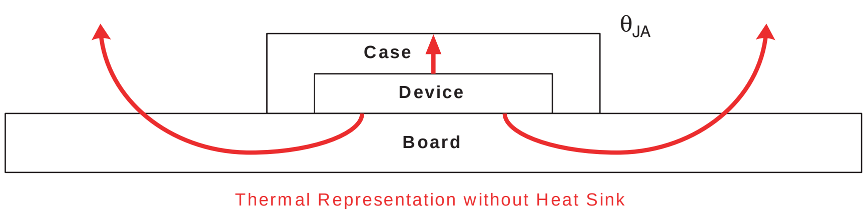
The device can be considered a heat source and the junction temperature is the temperature at the device. For simplicity, assume that the temperature of the device is constant regardless of where it is being measured. In reality, the temperature varies across the device.

Power can be dissipated from the device through many paths. Different paths become significant depending on the thermal properties of the system. In particular, the significance of power dissipation paths vary depending on whether or not a heat sink is used for the device.

Not Using a Heat Sink

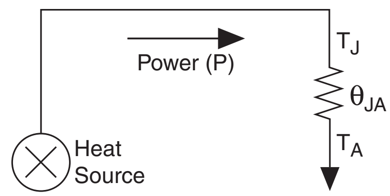
When a heat sink is not used, the major paths of power dissipation are from the device to the air. This can be referred to as a junction-to-ambient thermal resistance (θ_{JA}). In this case, there are two significant junction-to-ambient thermal resistance paths. The first is from the device through the case to the air. The second is from the device through the board to the air. Figure 3–15 shows the thermal representation without a heat sink.

Figure 3–15. Thermal Representation without a Heat Sink



In the model used in the PowerPlay Early Power Estimator, power is dissipated through the case and board. Values of θ_{JA} have been calculated for differing air flow options accounting for the paths through the case and through the board. Figure 3–16 shows the thermal model for the PowerPlay Early Power Estimator without a heat sink.

Figure 3–16. Thermal Model in the PowerPlay Early Power Estimator without a Heat Sink



The ambient temperature does not change, but the junction temperature changes depending on the thermal properties. Because a change in junction temperature affects the thermal device properties used to calculate junction temperature, calculating junction temperature is an iterative process.

The total power is calculated based on the θ_{JA} and the ambient, and junction temperatures using Equation 3–1:

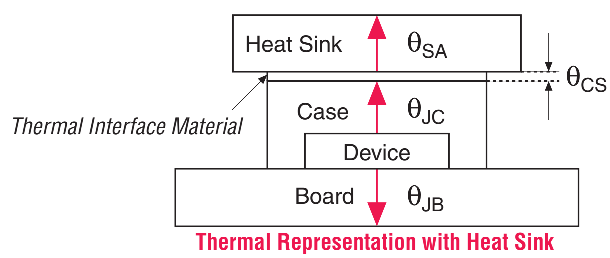
Equation 3–1.

$$P = \frac{(T_J - T_A)}{\theta_{JA}} + \frac{(T_J - T_B)}{\theta_{JB}}$$

Using a Heat Sink

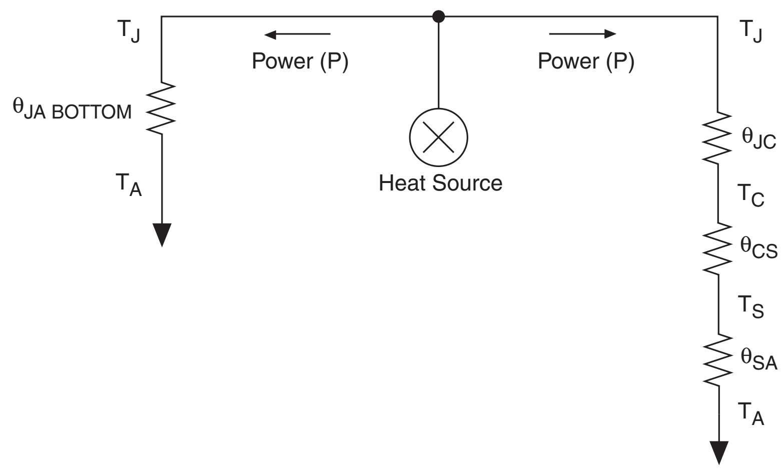
When a heat sink is used, the major paths of power dissipation are from the device through the case, thermal interface material, and heat sink. There is also a path of power dissipation through the board. The path through the board has much less impact than the path to air. Figure 3–17 shows the thermal representation with a heat sink.

Figure 3–17. Thermal Representation with a Heat Sink



In the model used in the PowerPlay Early Power Estimator, power can be dissipated through the board or through the case and heat sink. The thermal resistance of the path through the board is referred to as the junction-to-board thermal resistance ($\theta_{JA\ BOTTOM}$). The thermal resistance of the path through the case, thermal interface material, and heat sink is referred to as the junction-to-ambient thermal resistance ($\theta_{JA\ TOP}$). Figure 3–18 shows the thermal model for the PowerPlay Early Power Estimator.

Figure 3–18. Thermal Model for the PowerPlay Early Power Estimator with a Heat Sink



If you want the PowerPlay Early Power Estimator spreadsheet thermal model to take the junction-to-ambient bottom thermal resistance into consideration, set the Board Thermal Model to either **JEDEC (2s2p)** or **Typical Board**. If you do not want the PowerPlay Early Power Estimator spreadsheet thermal model to take the $\theta_{JA\ BOTTOM}$ resistance into consideration, set the Board Thermal Model to **None (conservative)**. In this case, the path through the board is not considered for power dissipation and a more conservative thermal power estimate is obtained.

The junction-to-ambient thermal resistance ($\theta_{JA\ TOP}$) is determined by the addition of the junction-to-case thermal resistance (θ_{JC}), the case-to-heat sink thermal resistance (θ_{CS}) and the heat sink-to ambient thermal resistance (θ_{SA}).

Equation 3–2.

$$\theta_{JA\ TOP} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

Based on the device, package, airflow, and heat sink solution selected in the main input parameters, the PowerPlay Early Power Estimator spreadsheet determines the junction-to-ambient thermal resistance ($\theta_{JA\ TOP}$).

If you are using a low, medium, or high profile heat sink, select the airflow from the options of still air and air flow rates of 100 lfm (0.5 m/s), 200 lfm (1.0 m/s), and 400 lfm (2.0 m/s). If you are using a custom heat sink, enter the heat sink-to-ambient thermal resistance (θ_{SA}). The airflow should also be incorporated into θ_{SA}. Therefore, the Airflow parameter is not applicable in this case. Obtain these values from the heat sink manufacturer.

The ambient temperature does not change, but the junction temperature changes depending on the thermal properties. Because a change in junction temperature affects the thermal device properties used to calculate junction temperature, calculating junction temperature is an iterative process.

The total power is calculated based on the total θ_{JA}, and the ambient, and junction temperature using Equation 3–3:

Equation 3–3.

$$P = \frac{(T_J - T_A)}{\theta_{JA}}$$

Figure 3–19 shows the thermal analysis, including the junction temperature (T_J), total θ_{JA}, and the maximum allowed T_A values. For details on the values of the thermal parameters not listed, click the **Details** button.

Figure 3–19. Thermal Analysis in the PowerPlay Early Power Estimator

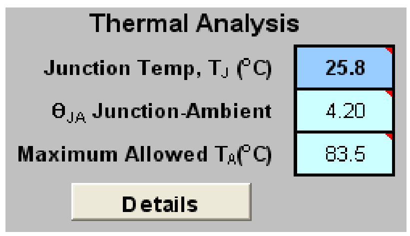


Table 3–13 describes the thermal analysis parameters in the PowerPlay Early Power Estimator.

Table 3–13. Thermal Power Section Information

Input Parameter	Description
Junction Temp, T_J (°C)	This shows the device junction temperature estimated based on supplied thermal parameters. The junction temperature is determined by dissipating the total thermal power through the top of the chip and through the board (if selected). See **Details** for detailed calculations used.
θ_{JA} Junction-Ambient	This shows the junction-to-ambient thermal resistance between the device and ambient air (in °C/W). This represents the increase in temperature between ambient and junction for every Watt of additional power dissipation.
Maximum Allowed T_A (°C)	This shows a guideline for the maximum ambient temperature (in °C) that the device can be subjected to without violating maximum junction temperature, based on the supplied cooling solution and device temperature grade.

Power Supply Current (A)

The power supply current section provides the estimated current draw from all power supplies. The I_{CC} /I_{CCCB} /I_{CCA_PLL}/I_{CCD_PLL} current is the supply current required from V_{CC} /V_{CCCB} /I_{CCA_PLL} /I_{CCD_PLL}, respectively. The total I_{CCPD} current is the supply current required from all V_{CCPD} power supplies. The total I_{CCIO} current is the supply current required from all V_{CCIO} power supplies. For estimates of I_{CCPD} and I_{CCIO} based on power supply, refer to "General I/O Pins" on page 3–12. The total ICCXCVR current is the supply current required from all transceiver power supplies. For estimates of ICCXCVR based on power supply, refer to "Transceiver (XCVR)" on page 3–21.

Figure 3–20 shows the power supply current estimation. I_{CC}, I_{CCCB}, I_{CCA_PLL}, I_{CCD_PLL}, I_{CCPD} and I_{CCIO} are displayed.

Figure 3–20. Power Supply Current in the PowerPlay Early Power Estimator

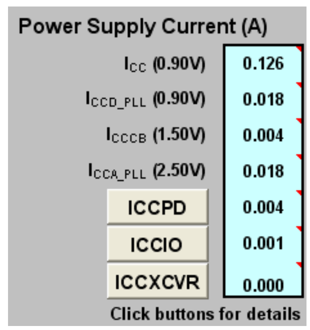


Table 3–14 describes the parameters in the **Power Supply Current** section of the PowerPlay Early Power Estimator.

Table 3–14. Power Supply Current Information

Input Parameter	Description
I_{CC}	This shows the total current drawn from the V_{CC} supply (in A).
I_{CCCB}	This shows the total current drawn from the V_{CCCB} supply (in A).
I_{CCA_PLL}	This shows the total current drawn from the I_{CCA_PLL} supply (in A).
I_{CCD_PLL}	This shows the total current drawn from the I_{CCD_PLL} supply (in A).
I_{CCPD}	This shows the total current drawn from the V_{CCPD} power rail(s). See the **I/O sheet** for details on the current drawn from each power rail.
I_{CCIO}	This shows the total current drawn from the V_{CCIO} power rail(s). See the **I/O sheet** for details on the current drawn from each power rail. I_{CCIO} includes any current drawn through the I/O into off-chip termination resistors. This can result in I_{CCIO} values that are higher than the reported I/O thermal power because this off-chip current is dissipated as heat elsewhere and does not factor into the calculation of device temperature.
I_{CCXCVR}	This shows the total current drawn from the I_{CCXCVR} power rail(s). See the **XCVR sheet** for details on the current drawn from each power rail.

For more information regarding power supplies, refer to the *Datasheet* chapter in volume 3 of the *Arria II GX Device Handbook*.

Factors Affecting PowerPlay Early Power Estimator Spreadsheet Accuracy

There are many factors that greatly affect the estimated values displayed in the PowerPlay Early Power Estimator. In particular, it is imperative to determine whether or not the input parameters entered are accurate to ensure that the system is modeled correctly in the PowerPlay Early Power Estimator spreadsheet. Information entered concerning toggle rates, airflow, temperature, and heat sinks are extremely important.

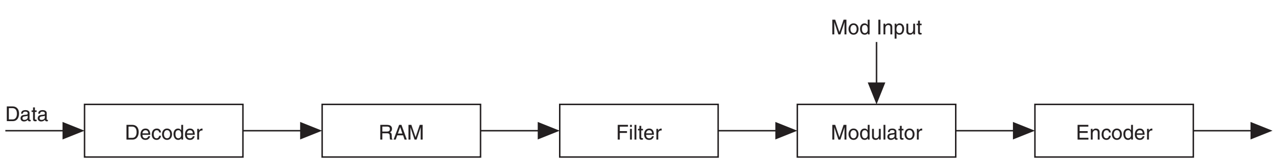
Toggle Rate

The toggle rates specified in the PowerPlay Early Power Estimator spreadsheet can have a very large impact on the dynamic power consumption displayed. In order to obtain an accurate estimate, it is imperative to input toggle rates that are realistic. Determining realistic toggle rates is a major concern that requires the designer to know what kind of input the FPGA is receiving and how often it toggles.

If the design is not yet complete, it is very difficult to get an accurate estimate. The best way to approach the problem is to isolate the separate modules in the design by functionality and estimate resource usage along with toggle rates of the resources. The easiest way to accomplish this is to leverage previous designs to estimate toggle rates for modules with similar functionality.

As an example, assume that there is a simple design that has an input data bus encoded for data transmission and has a roughly 50% toggle rate. It then goes through a decoder and is stored in RAM. The data is then filtered before being modulated with another input data bus and the result is encoded for transmission. A simple block diagram is shown in Figure 3–21.

Figure 3–21. Decoder and Encoder Block Diagram



In this case you would have to estimate the following:

- Data toggle rate
- Mod input toggle rate
- Resource estimate for Decoder module
- Resource estimate for RAM
- Resource estimate for Filter
- Resource estimate for Modulator
- Resource estimate for Encoder
- Toggle rate for Decoder module
- Toggle rate for RAM
- Toggle rate for Filter

- Toggle rate for Modulator
- Toggle rate for Encoder

These estimates can be done in many ways. If similar modules were used in the past with data inputs of roughly the same toggle rate, you can leverage that information. If there are MATLAB simulations available for some blocks, you can obtain the toggle rate information. If the HDL is available for some of the modules, you can simulate them.

If the HDL is complete, the best way to determine toggle rate is to simulate the design. The accuracy of toggle rate estimates depends heavily on the accuracy of the input vectors. Therefore, determining whether or not the simulation coverage is high gives you a good estimate of how accurate the toggle rate information is.

The Quartus II software can determine toggle rates of each resource used in the design if you provide information from simulation tools. Designs can be simulated in many different tools and information provided for the Quartus II software through a signal activity file (**.saf**). The Quartus II PowerPlay Power Analyzer provides the most accurate power estimate. You can import the comma-separated value file (**.csv**) from the Quartus II software into the PowerPlay Early Power Estimator spreadsheet for estimating power after the design is complete.

Airflow

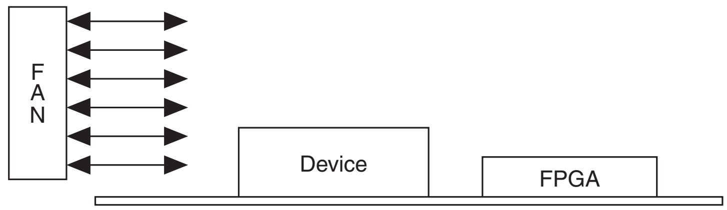
The PowerPlay Early Power Estimator spreadsheet allows you to specify the airflow present at the device. This value affects thermal analysis and can significantly affect the power consumed by the device. To obtain an accurate estimate, it is imperative to correctly determine the airflow at the FPGA, not the output of the fan providing the airflow.

Often it is difficult to place the device adjacent to the fan providing the airflow. As such, the path of the airflow is likely to traverse a length on the board before reaching the device, thus diminishing the actual airflow the device sees. In the example below (Figure 3–22), a fan is placed at the end of the board. The airflow at the FPGA is weaker than what it is at the fan.

Figure 3–22. Airflow and FPGA Positon

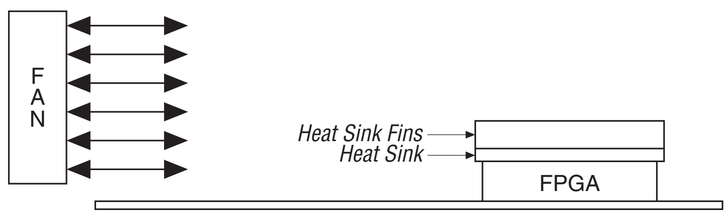
In many cases, it is also necessary to take into consideration blocked airflow. In the example below (Figure 3–23), there is a device blocking the airflow from the FPGA, significantly reducing the airflow seen at the FPGA. Also, the airflow from the fan often cools board components and other devices before reaching the FPGA.

Figure 3–23. Airflow with Component and FPGA Positions



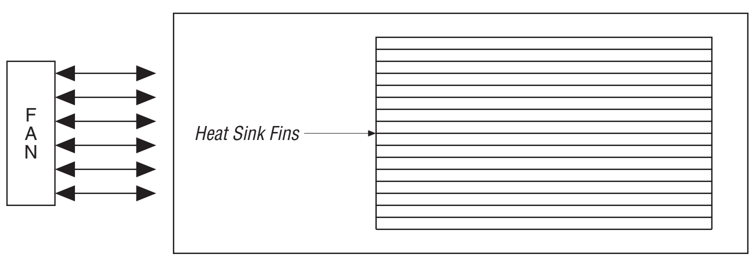
If you are using a custom heat sink, there is no need to enter the airflow value directly into the PowerPlay Early Power Estimator spreadsheet, but it is required to compute the θ_{SA} for the heat sink with the information of what the airflow is at the device. Most heat sinks have fins located above the heat sink to facilitate airflow. Figure 3–24 shows the case of an FPGA with a heat sink.

Figure 3–24. AirFlow and Heat Sinks



When placing the heat sink on the FPGA, it is imperative that the direction of the fins correspond with the direction of the airflow. A top view shows the correct orientation of the fins (Figure 3–25).

Figure 3–25. Heat Sink (Top View)



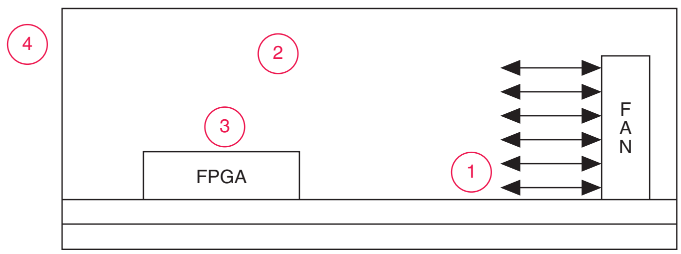
The considerations above can heavily influence the airflow seen at the device. When entering information into the PowerPlay Early Power Estimator spreadsheet, it is necessary to consider these implications in order to get an accurate airflow value. It is your responsibility to determine the actual airflow at the FPGA and correctly input this value into the PowerPlay Early Power Estimator spreadsheet.

Temperature

The PowerPlay Early Power Estimator spreadsheet requires you to enter the ambient air temperature for the device in order to calculate the device's thermal information correctly. Ambient temperature refers to the temperature of the air around the device. This is almost always much higher than the ambient temperature outside of the system. To get an accurate representation of ambient temperature for the device, the temperature must be measured as close to the device as possible. This can be done with a thermocouple.

Entering the incorrect ambient air temperature could drastically alter the power estimates in the PowerPlay Early Power Estimator spreadsheet. Figure 3–26 below illustrates a simple system with the FPGA housed in a box. In this case, the temperature is very different at each of the numbered locations.

Figure 3–26. Temperature Variances



For example, location 3 is where the ambient temperature pertaining to the device should be obtained for input into the PowerPlay Early Power Estimator spreadsheet. Points 1 and 2 are cooler than location 3 and location 4 is likely close to 25°C. Temperatures close to devices in a system are often in the neighborhood of 50-60°C but the values can vary significantly. In order to obtain accurate power estimates from the PowerPlay Early Power Estimator spreadsheet, it is very important to get a realistic estimate of the ambient temperature near the FPGA device.

Heat Sink

When using a heat sink, the power is determined by the two equations in Equation 3–4:

Equation 3–4.

$$\frac{(T_J - T_B)}{\theta_{JB}} = P$$

$$\theta_{JA\ TOP} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

The value θ_{JC} is specific to the FPGA and can be obtained from the data sheet. The value θ_{CS} refers to the material that binds the heat sink to the FPGA and is approximated to be 0.1 °C/W. The value θ_{SA} is obtained from the manufacturer of the heat sink. It is important to ensure that when this value is obtained that it is for the right conditions for the FPGA, which include analyzing the correct heat sink information at the appropriate airflow at the device.

For more information about how to determine heat sink values, refer to *AN 358: Thermal Management for 90-nm FPGAs* and the Altera website (www.altera.com). The information contained in the application note is also applicable to 65-nm and 40-nm FPGAs.

Document Revision History

The table below displays the revision history for the chapters in this User Guide.

Date	Document Version	Changes Made
March 2009	1.0	Initial release

Referenced Documents

This user guide references the following documents:

- *AN 358: Thermal Management for 90-nm FPGAs*
- *Arria II GX Device I/O Features* chapter in volume 1 of the *Arria II GX Device Handbook*
- *DSP Blocks in Arria II GX Devices* chapter in volume 1 of the *Arria II GX Device Handbook*
- *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*

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	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Non-technical support (General)	Email	nacomp@altera.com
Non-technical support (Software Licensing)i	Email	authorization@altera.com

Note to table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, file names, file name extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input`. Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
	The hand points to information that requires special attention.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or the user's work.
	A warning calls attention to a condition or possible situation that can cause injury to the user.
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.