

A Flexible Architecture to Drive Sharp Two-Way Viewing Angle and Standard LCDs

Introduction

One of the most common elements in today's consumer and automotive electronics is the liquid crystal display (LCD). LCD technology has produced a large array of products that meet a wide range of size, power, and image quality requirements. Recent innovation from Sharp Electronics goes one step further with the development of a two-way viewing angle LCD product.

The popularity of standard LCDs has led to a number of semiconductor solutions to drive them, ranging from ASSPs to full-custom devices. These devices are fixed-function solutions that can restrict the options of product developers who need either a flexible solution to support the needs of specific applications, or a scalable solution to support multiple, similar applications as in the case of a product line or family. In the case of two-way viewing LCD products, no standard driver solution exists, so a custom solution is required to support them. This paper discusses an innovative architecture based on FPGAs and soft-core embedded processors that supports both standard and two-way viewing LCD products.

Traditional Solutions for Driving LCDs

Traditional LCD solutions are hampered by limitations including multiple simultaneous displays, different display types, nonstandard or very high resolutions, changing requirements, extended product lifespans, and support for memory standards.

Multiple simultaneous displays: For some applications it is desirable to drive several different displays simultaneously, either with identical or different image content. These displays may also have varied resolutions; most display drivers are not equipped to support this.

Different display types: For applications where both two-way viewing and standard LCDs are present, traditional solutions require separate devices to drive each LCD type, which is inefficient. Since creating ASSPs and full-custom devices requires large up-front investments and long development times, a fixed-function device to support both display types is not yet available and may not be for some time.

Non-standard or very high resolutions: Fixed-function display driver devices can only support the resolutions for which they were designed, limiting the ability of product developers to differentiate their products with nonstandard or very high resolutions.

Changing requirements over the lifetime of the product: A product developer might want to support different image content over the lifetime of the product, including different resolutions, 3D graphics, new video formats, etc., which is impossible with fixed-function devices.

Extended product lifespans: Many products using LCDs, such as those in automotive applications, must be manufacturable for many years. Despite this, ASSP and custom device vendors can obsolete their products at any time (sometimes as soon as 18 months after introduction), often when the market for their product has become less desirable, or when they lose major customers. This obsolescence creates significant manufacturing difficulties for the remaining customers.

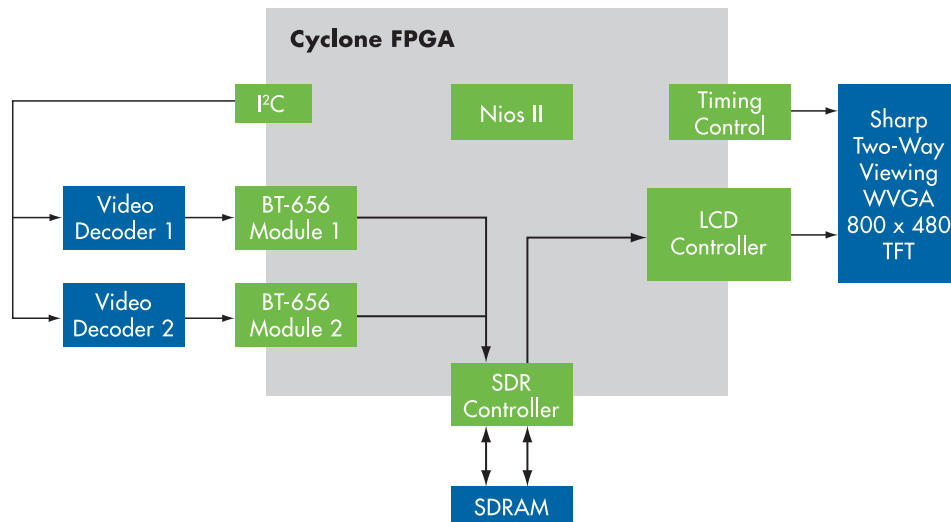
Memory standard support: Fixed-function LCD drivers generally support only one memory standard, such as SDRAM. This limitation prevents product developers from using different memory types to achieve higher performance or a different price/performance ratio.

FPGA-Based LCD Driver Architecture

The limitations of fixed-function devices for driving LCD panels can be overcome by replacing them with a combination of FPGAs and soft-core processor solutions. The flexible nature of FPGAs supports a variety of LCD panel requirements. For example, many different memory standards are supported by using the appropriate memory controllers. FPGA reconfigurability also allows designers to change the LCD driver functionality after the product has been manufactured, enabling easy in-field product upgrades or enhancements. By utilizing a soft-core processor development environment, designers can quickly and efficiently assemble the elements needed to drive a wide range of LCD panel configurations for implementation within an FPGA.

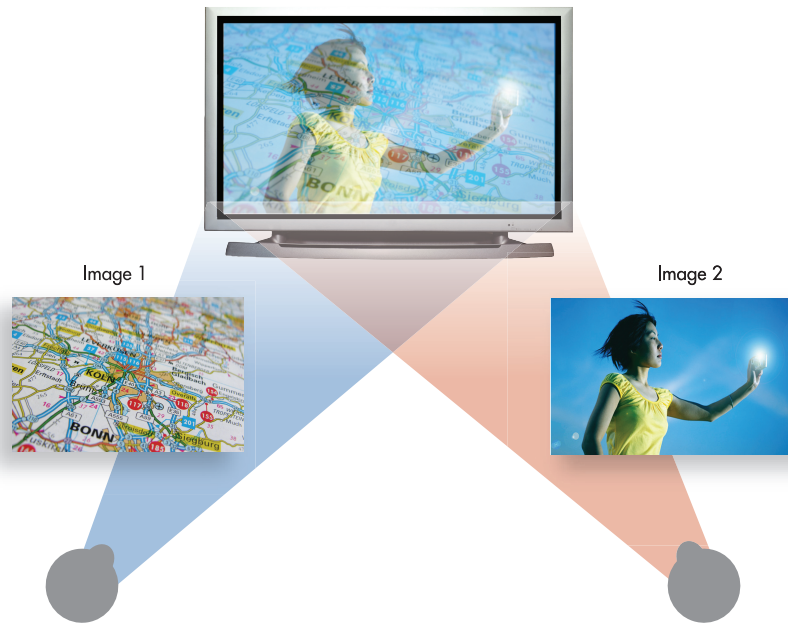
Altera provides an LCD driver architecture that, for the first time, addresses design challenges of both standard and two-way viewing LCD products while enabling product developers and manufacturers to choose from several devices, based on their needs and without concern about semiconductor component obsolescence. This architecture utilizes devices from the Altera® Cyclone® FPGA series and Nios® II soft-core embedded processors, and is based on five modules. The five modules, defined by their corresponding function, are two BT-656 video inputs, an LCD control, an SDRAM control, and an I²C control. The processor performs the overall control and arbitration of the system. When employed in a Cyclone series FPGA and connected via the Avalon® bus, these modules provide all of the necessary throughput and video bandwidth to drive a two-way viewing LCD panel with 800x480 resolution. A block diagram of a sample system is shown in [Figure 1](#).

Figure 1. FPGA-Based LCD Driver System Block Diagram



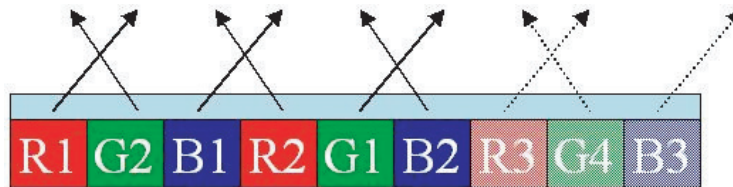
To further describe the elements of the Altera FPGA-based LCD driver architecture, it will be useful to understand how the two-way viewing LCD panel operates in comparison to a standard LCD panel. This intriguing technology allows simultaneous display of two independent images on the same physical glass surface of the LCD. The images are not shown side-by-side or picture-in-picture, but rather concurrently, separated by two optical viewing cones: one for viewing from the right and one for viewing from the left (shown in [Figure 2](#)). For example, in an automotive application, a car's driver viewing the display from the left might see the dashboard instruments or navigation information, while a passenger viewing the display from the right can watch a movie; both images would appear across the full surface of the display.

Figure 2. Two-Way Viewing Angle LCD Produces Two Viewing Cones



Electrically, a two-way viewing LCD panel is identical to a standard LCD panel. As with a standard LCD panel, data is written to the display in a row-column pixel matrix that traverses the display from left to right and top to bottom. Additionally, both timing and synchronization signals remain identical to standard glass LCDs. The dual image effect is derived by physical means. Above the liquid crystal material is an optical director layer (the light blue bar shown in Figure 3) that routes light from the subpixels to each independent field of view.

Figure 3. Optical Direction of Subpixel Information

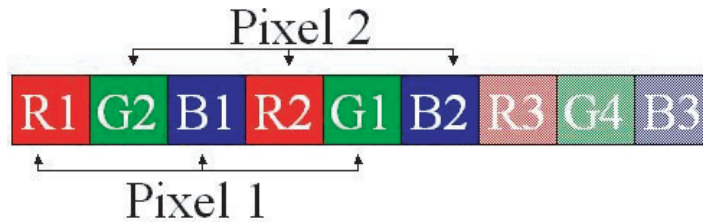


Since the optical director is static, it relies on the organization of the subpixel data beneath it for proper image creation and alignment. Therefore, reorganization and mixing of the subpixel data must occur prior to the data being written to the display (shown in Figure 4). In a two-way viewing LCD panel, shown in Figure 5, the subpixels of one image alternate with subpixels from the other, as denoted by the numbers in the diagram. Since two images are “woven” together, they divide the effective display resolution in the horizontal direction. For example, if the total resolution of the display is 800x480, each viewable image would be 400x480. To the observer, the resolution difference is negligible since the image is stretched across the entire horizontal dimension of the display.

Figure 4. Subpixel Organization on a Standard LCD



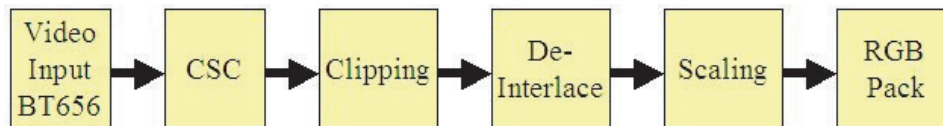
Figure 5. Subpixel Organization on a Two-Way Viewing LCD



BT-656 Video Input Module

The BT-656 video input module (shown in Figure 6) is designed to be compatible with the ITRU-BT656 digital video standard. This module is responsible for the following operations: color space conversion (CSC), clipping, de-interlacing, scaling, and an RGB 565 pack. Each operation is performed sequentially and is parameterized by registers controlled by a Nios II processor. Optionally, the video inputs may be clipped and scaled (up or down) depending on the desired output format. The registers allow the system to be customized for various display resolutions and input video formats such as NTSC, PAL, or SECAM. Video data from the module is transferred via a 32-bit direct memory access (DMA) to an external SDRAM frame buffer. The pixel data is packed to a RGB 565 format, transferring two pixels as one word during the DMA. This greatly increases video bandwidth and overall efficiency of memory access.

Figure 6. BT-656 Video Input Module



The system block diagram in Figure 1 shows two BT-656 video input modules, as these enable two video input sources for the system. Alternatively, the second video path could be replaced with another digital source such as a digital RGB output from an automotive navigation system. Additional BT-656 video input modules are possible if desired; the only limitation on the number of modules is the available FPGA resources.

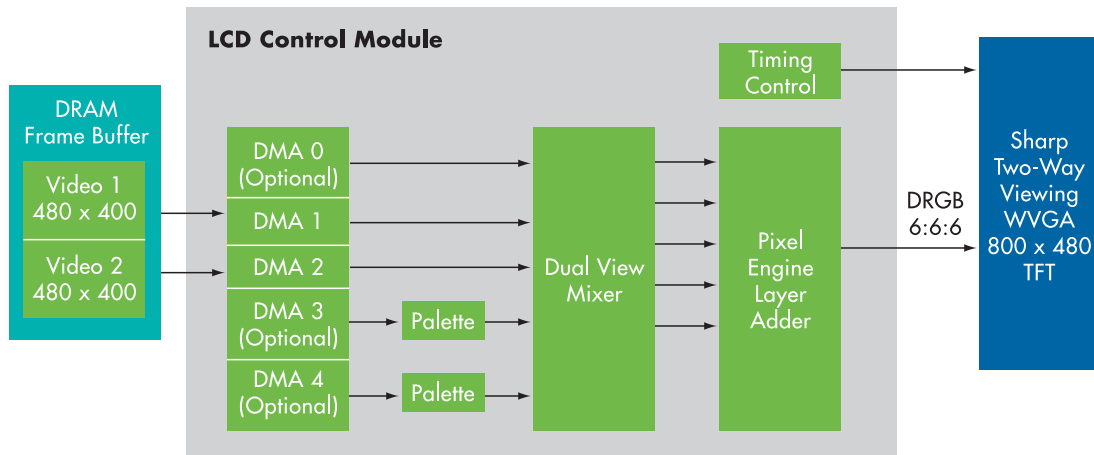
As an example, consider a two-way viewing LCD panel with an 800x480 resolution. This resolution requires that both sources must be scaled to 400x480. The video module is responsible for all image scaling within the system. By referring to register and control settings from the Nios II processor, the video module precisely sets the desired output frame resolution. The resulting video frames from each source are then individually buffered within the DRAM (see Figure 7).

One of the key system considerations is memory bandwidth. If the system is designed with double data rate (DDR) RAM (or equivalent), additional input data paths may be possible. However, additional DDR requires additional internal bus width (e.g., adding 32-bit DDR creates a 64-bit wide internal bus). This memory bandwidth requires more FPGA resources, which can be accommodated by selecting the appropriate FPGA device.

LCD Controller Module

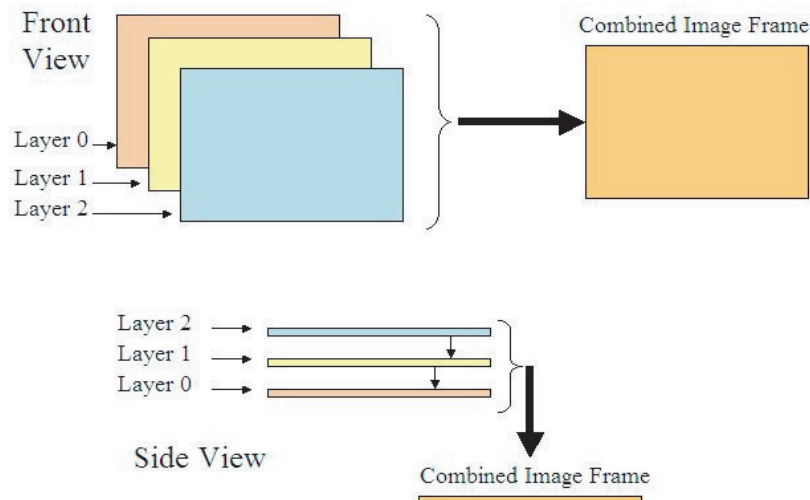
The LCD controller module is a multilayer LCD controller containing three 16-bit color image layers and, optionally, two 8-bit palette layers (see Figure 7). Each layer is formed and controlled by a separate DMA master, thus creating efficient partitioning of the external DRAM-based frame buffer. Therefore, each DMA master may read from the frame buffer whenever it requires data, enabling the LCD controller module to read any frame resolution or image size stored in the external memory.

Figure 7. LCD Control Module Block Diagram



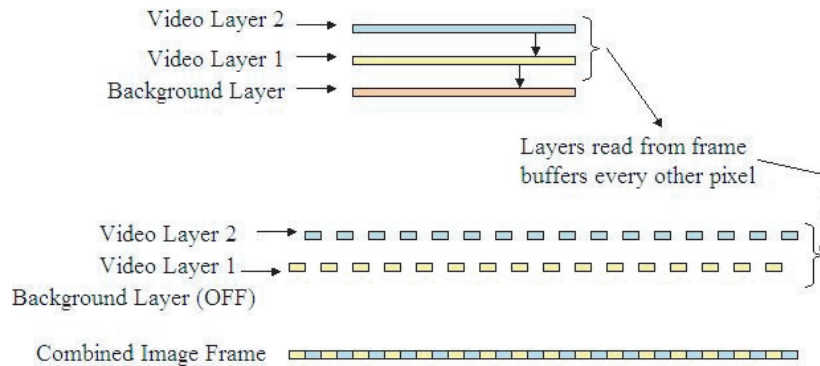
As each layer master reads from memory, the LCD controller module combines (or flattens) the layers into one combined frame. This combined frame is then sent to the LCD (see Figure 8). As the LCD controller module combines the layers, it can apply an alpha value or transparency factor to each (with the exception of the background layer, layer 0). Additionally, each layer may be completely turned on or off, enabling layers to be activated or deactivated as desired.

Figure 8. Layer Combination or Flattening



The finite layer control is one of the means of controlling the two-way viewing LCD panel. Each video source is routed to separate and equally dimensioned frame buffers. As an example, consider again a two-way viewing LCD panel with 800x480 resolution. This output resolution defines that each video frame must be sized to 400x480, but for timing and synchronization purposes, the LCD controller is set to control the full resolution of 800x480. To construct the two-way viewing image, the DMA controllers of the two video layers grab alternating pixels from their frame buffers. Each video layer then effectively consists of data at every other pixel location. The layers are offset from each other by one pixel and then flattened into one layer for the output image frame (see Figure 9). This process preserves the overall display timing parameters and enables the FPGA to weave the pixel information together.

Figure 9. Dual-View Layer Construction



Resource Utilization and Implementation

The FPGA-based LCD driver architecture easily scales to support LCD panels of various sizes, both standard and two-way viewing. Additional capabilities, such as customized on-screen displays, splash screens, graphics acceleration, 3D rendering, or support for any number of LCD panels can be included by adding functionality to the FPGA design and selecting the appropriately sized FPGA for implementation.

Product developers gain not only design flexibility when using an FPGA-based architecture, but also cost effectiveness without sacrificing performance. For example, the FPGA elements shown in [Figure 1](#) utilize approximately 12K logic elements (LEs) of a Cyclone II FPGA, which is less than 70 percent of an EP2C20 Cyclone II device. The EP2C20 Cyclone II devices cost less than \$10 in volume production quantities of 500K units, yielding an implementation cost of about US\$7. In a Cyclone III device, the same design occupies about 9K LEs, yielding an implementation cost of less than US\$4.

Jabil Implementation

Jabil Circuit, Inc. recognized that the automotive industry's traditional point solutions for driving LCDs did not fit its electronics manufacturing services (EMS) business model. To achieve the economies of scale needed to provide customers with the best-priced solution, Jabil created a flexible, scalable display system using the Altera-based LCD driver architecture. The Jabil architecture uses variations of the system shown in [Figure 1](#) to effectively drive multiple sizes and versions of Sharp's digital LCDs, up to and including the two-way viewing-angle LCD.

While the variations required to support the many different displays are made by modifying the design programmed into the Altera FPGA, different customer requirements (video input types, backlight driver circuitry, etc.) demand a simple yet sophisticated hardware strategy. To this end, Jabil analyzed the current and future trends in the LCD market, and created a population/depopulation strategy that uses the core architecture while allowing easy modification of the specific hardware to satisfy customer and LCD requirements. This design, which fits within the 7" LCD form factor, allows Jabil to cost-effectively manufacture variations on the base designs.

Using the Altera-based LCD driver architecture, Jabil created three ascending variations: Base, High Content, and Two-Way viewing. These include all of the video presentation components required for automotive entertainment and information systems. The scalability of the Jabil architecture and the Cyclone FPGA family enables different cost/functionality tradeoffs to be made as the functionality requires, thus minimizing component costs.

The Jabil Base Rear Seat Entertainment (RSE) module is intended for headrest- and ceiling-mounted video playback. The module is compatible with vehicle systems requiring processing and display of Composite Video Baseband Signals (CVBS). A cold cathode fluorescent lamp (CCFL) provides variable brightness adjustment of the LCD backlight as indicated by a pulse width modulated (PWM) input. Both NTSC and PAL video formats are supported, and are autodetected or manually indicated by the video mode PWM input. Multiple video scaling modes are also

supported. An automotive-compliant power supply insures reliable operation and compatibility with the vehicle environment.

The High Content module is compatible with vehicle systems requiring processing and display of composite or component video. These can be located either in an RSE location or the center stack. Compatible video formats include composite NTSC, composite PAL, S-Video NTSC, and analog RGB. Composite NTSC and PAL video formats are autodetected or manually controlled. The scaling engine is used to achieve multiple video frame sizes, and alpha blending is supported for transparency and fading of displayed content. Frame buffers enable de-interlacing by either bobbing or weaving methods. A communication network provides remote command of user-adjusted settings. Options include single wire CAN, dual wire CAN, and LIN or UART interface, all of which support module reprogramming.

An on-screen display (OSD) processor can be developed using a PC-based tool, and downloaded into the Altera FPGA. This processor enables graphical feedback of user-adjusted control settings, with menus that are navigated remotely over the communication network. Control settings and custom graphic screens for display at power up or during the absence of video inputs are stored in nonvolatile memory, with internal module diagnostics offering verification of operational status.

The Jabil Two-Way viewing module is a video presentation component enabling multiple passengers to view separate video content from a single module. A two-way viewing LCD panel presents alternate video streams to the left and right viewing perspectives. The parallel channels are assignable to either viewing perspective, and single-view emulation is also supported by integrating the same image into both perspectives. Both NTSC and PAL CVBS are supported. The two-way viewing module can be manufactured with optional auxiliary RGB decoder or RGB deserializer, and parallel logic or LVDS are available for YCrCb and RGB parallel digital formats. The video formats, scaling, alpha blending, frame buffers, communication networks, nonvolatile memory, and OSD support found in the high content architecture are also supported in this architecture.

Analysis by Jabil comparing traditional LCD driver solutions versus the Jabil architecture has found that the bill of material (BOM) costs of the Jabil solution compare favorably to traditional solutions. By creating these base architecture references, Jabil helps customers save money. Instead of making large NRE investments, now the only NRE costs are spent on unique features customers may wish to add to their designs. Currently, Jabil has specifications and data validation (DV)-ready parts available for all three versions of the architecture.

Conclusion

Using Altera FPGA and soft-core embedded processor technology, the first LCD panel driver architecture that supports both two-way viewing LCD panels and standard LCD panels has been developed. This scalable and flexible architecture overcomes many of the shortcomings of traditional LCD driver solutions. The architecture's Nios II processor is versatile and powerful enough to take on additional embedded processor functions. Additionally, using the Nios II processor to reduce or eliminate the need for off-the-shelf embedded processors allows further efficiencies and cost savings.

Further Information

- *Sharp to Mass Produce World's First LCD to Simultaneously Display Different Information in Right and Left Viewing Directions:*
http://www.sharp-world.com/corporate/news/050714_2.html

Acknowledgements

- Brian Petku, Senior Field Technical Manager, Sharp Microelectronics of the Americas, Sharp Corporation
- Dave Anderson, Field Applications Manager, Trilogy Marketing
- Pat Hourigan, Technical Marketing Manager, Jabil Circuit
- Martin S. Won, Senior Member of Technical Staff, Altera Corporation
- Roger May, Manager AIM Systems Solutions Group, Altera Corporation

JABIL SHARP



101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
<http://www.altera.com>

Copyright © 2007 Altera Corporation. All rights reserved. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations, and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. All other product or service names are the property of their respective holders. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.