
Using Cyclone III FPGAs for Emerging Wireless Applications

Introduction

Emerging wireless applications such as remote radio heads, pico/femto base stations, WiMAX customer premises equipment (CPE), and software defined radio (SDR) have stringent power consumption and low cost requirements. In addition to these challenges, given the high data rate requirements and ever-evolving standards, designers also need to ensure high performance and flexibility in the end products.

This paper gives an overview of how Altera® Cyclone® III FPGAs address the diverse requirements for wireless applications, with the WiMAX pico base station discussed as a case study.

Emerging Wireless Applications

Market needs for higher data rates are driving the evolution of wireless cellular systems from narrowband 2G GSM IS-95 systems to current-generation W-CDMA-based 3G and 3.5G systems supporting peak data rates up to 10 Mbps. For future 3GPP long-term evolution specifications, complex signal processing techniques such as multiple-input multiple-output (MIMO), along with new radio technologies like OFDMA, are considered key to achieving target throughputs in excess of 100 Mbps. Alternate OFDM-based broadband wireless systems such as WiMAX have similarly evolved, achieving transmission speeds in excess of 70 Mbps. In-building coverage is also regarded as a key requirement for future wireless growth, with technologies such as pico and femto base stations trying to address this issue. Remote radio heads is another emerging technology aimed at improving coverage while reducing capital and operating expenditures.

Design Requirements for Emerging Applications

The emerging wireless technologies described above pose significant challenges for OEMs needing to design products that are not only scalable and cost-effective but also flexible and reusable across multiple evolving standards. These diverse requirements ultimately drive the hardware platform choice.

Low-Cost Production

Systems such as pico base stations have significantly lower bills of materials (BOMs), typically in hundreds of dollars, as opposed to macro and micro base stations with BOM ranges in the thousands of dollars. Similarly, WiMAX CPE equipment is predicted to reach sub-US\$200 range. To support these price points, the underlying silicon should have low-cost, high-volume production capability.

Low Power Consumption

Systems such as pico base stations and remote radio heads have much smaller footprints than macro and micro base stations and are usually mounted on rooftops and poles. Due to the small form factor and weight requirement, these systems usually do not include forced air-flow or cooling fans, leading to stringent limitations on the permissible power consumption levels in the underlying hardware.

Flexibility

WiMAX is a relatively new market and is currently in the initial development and deployment stages. Similarly, 3GPP LTE is being defined, with numerous revisions to go before being finalized. In this current scenario, having a flexible and reprogrammable product is necessary to enable bug fixes, and also to provide a standards-agnostic or multi-protocol base station solution, which cannot be achieved by designing ASICs in the end product. Systems offering this flexibility significantly reduce the capital and operating expenditures for wireless infrastructure OEMs and operators while alleviating risks posed by constantly evolving standards.

High Performance

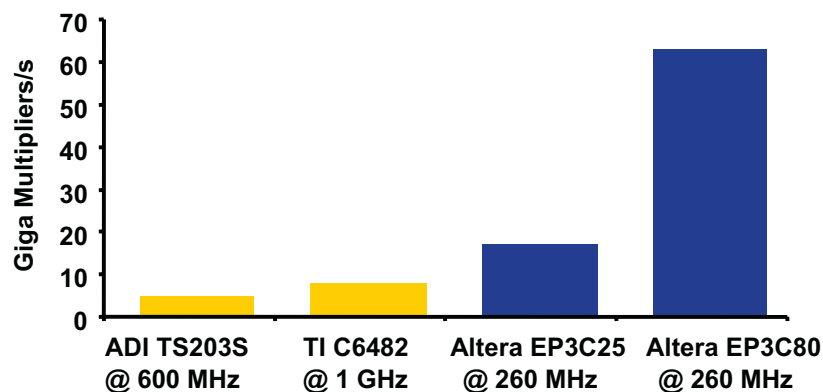
WiMAX broadband wireless systems have significantly higher throughput and data-rate requirements than W-CDMA and CDMA2000 cellular systems. To support these high data rates, the underlying hardware platform must have significant processing bandwidth. Additionally, several advanced signal-processing techniques, such as Turbo coding/decoding, and front-end functions, including fast Fourier transform/inverse fast Fourier transform (FFT/IFFT), are computationally intensive and require several billion multiply and accumulate (MAC) operations per second. Software programmable multipliers do not have the processing bandwidth to address these performance requirements and result in an inefficient cost-per-channel implementation.

Cyclone III FPGAs-Enabling Emerging Wireless Applications

Cyclone III FPGAs are equipped with an unprecedented combination of low power consumption, high functionality, and low cost to conserve system power, increase productivity, and maximize your competitive edge. With up to 3.9M bits of RAM, 120,000 logic elements (LEs), and 288 18 x 18 multipliers, the Cyclone III family provides a much higher level of functionality compared to any other low-cost FPGA.

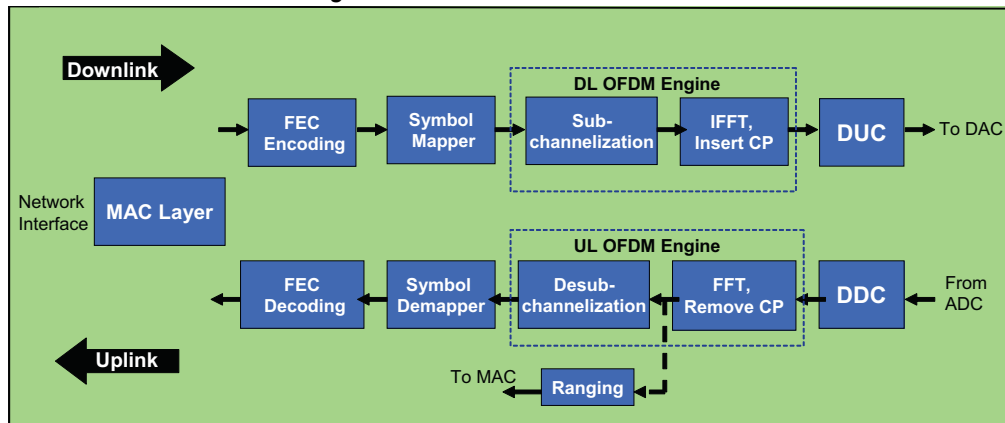
The Cyclone III family represents the pinnacle of Altera's leadership in offering the lowest power FPGAs. Combining a comprehensive approach of architecture and silicon enhancements, the latest semiconductor process technology, and complete power management tools for customers, Altera's efforts have resulted in an up to 50 percent reduction in power consumption compared to 90 nm-based Cyclone II FPGAs, and the lowest power consumption of any comparable FPGAs. Combine that large array of multipliers with on-chip memory and parallel processing capability, and Cyclone III FPGAs deliver significantly higher performance than off-the-shelf multipliers. [Figure 1](#) compares Cyclone III DSP performance to off-the-shelf multipliers.

Figure 1. Comparison of Cyclone III FPGA DSP Performance



[Figure 2](#) shows a block diagram of the functionality in a WiMAX pico base station. The following sections describe how the low power, memory, and multipliers of Cyclone III FPGAs can be used to implement various functions in the pico base station in a cost-efficient manner.

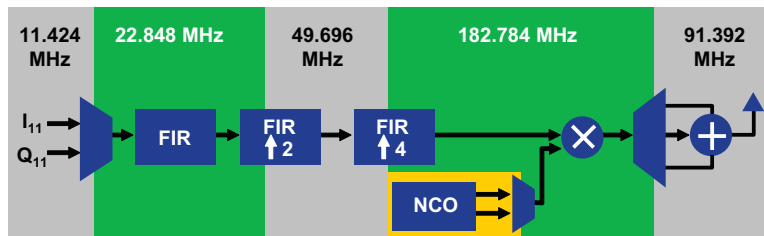
Figure 2. WiMAX Pico BTS Block Diagram



WiMAX DUC and DDC

Both digital upconverters (DUCs) and digital downconverters (DDCs) use complex filter architectures including finite impulse response (FIR) and cascaded integrator-comb (CIC) filters. Cyclone III FPGAs have up to 288 18x18 multipliers running at speeds as high as 260 MHz and provide a low-cost, low-power platform for implementing DUC and DDC functionality. Figure 3 and Figure 4 provide an overview of WiMAX DUC and DDC architectures and specifications.

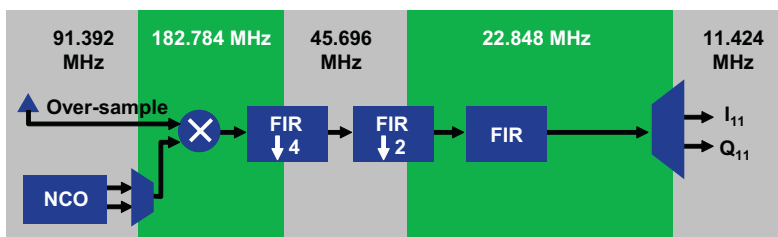
Figure 3. Single-Channel IQ Time-Division Multiplexed DUC



Note:

(1) NCO = Numerically controlled oscillator

Figure 4. Single-Channel IQ Time-Division Multiplexed DDC



More detailed information on the reference design can be found in *AN 421: Accelerating WiMAX DUC and DDC System Designs*: www.altera.com/literature/an/an421.pdf.

Table 1 lists the resources consumed in a Cyclone EP3C80 FPGA for these designs as well as for W-CDMA-based DUC and DDC pico base station designs. The Cyclone III EP3C80 implements DUC/DDC functions for WiMAX and W-CDMA applications using only a small percentage of resources, so the remaining FPGA can be used for the rest of the application.

Table 1. Resources of a Cyclone III EP3C80 FPGA Used for DDC/DUC

| | LUTs | Logic Registers | # of M9K Memories | 18 x 18 Multipliers | f _{MAX} (MHz) | Power (Watts) |
|------------------------------------|------|-----------------|-------------------|---------------------|------------------------|---------------|
| WiMAX DUC | 2704 | 5900 | 50 | 30 | 192 | 0.4 |
| WiMAX DDC | 2623 | 4786 | 46 | 25 | 203 | 0.4 |
| W-CDMA DUC | 4462 | 5865 | 28 | 18 | 149 | 0.3 |
| W-CDMA DCC | 4102 | 5666 | 21 | 22 | 144 | 0.3 |
| Maximum % of Used EP3C80 Resources | 6% | 7% | 28% | 10% | | |

Note:

(1) Power consumption is based upon pre-characterization estimates. These numbers will change once after final characterization.

An additional benefit seen in Table 1 is low power consumption, with DDC and DUC functions consuming less than 0.5 watts of power, and meeting power budgets for many new pico base stations and remote radio heads.

WiMAX OFDMA Engine

As seen in Figure 2, the downlink (DL) OFDMA engine includes the subchannelization, IFFT, and cyclic prefix insertion functions. Conversely, the uplink (UL) OFDMA engine includes cyclic prefix removal, FFT, and de-subchannelization functions. The abundant M9K memory blocks and multipliers in Cyclone III FPGAs enable a highly cost optimized implementation of the DL and UL OFDMA engines as seen in Table 2 and Table 3.

Table 2. Resources of a Cyclone III EP3C80 FPGA Used for DL OFDMA Engine

| FFT Size | Combinational ALUTs | Logic Registers | Memory (bits) | Memory M9K | Multipliers | | f _{MAX} (MHz) |
|----------|---------------------|-----------------|---------------|------------|-------------|---------|------------------------|
| | | | | | 9 x 9 | 18 x 18 | |
| 128 | 3,132 | 3,766 | 31,439 | 8 | 0 | 4 | 161 |
| 512 | 3,724 | 4,372 | 125,483 | 18 | 0 | 4 | 156 |
| 1,024 | 4,176 | 4,646 | 250,916 | 33 | 0 | 4 | 171 |
| 2,048 | 5,142 | 5,300 | 501,762 | 63 | 0 | 4 | 172 |

Table 3. Resources of a Cyclone III EP3C80 FPGA Used for UL OFDMA Engine

| FFT Size | Combinational ALUTs | Logic Registers | Memory (bits) | Memory M9K | Multipliers | | f _{MAX} (MHz) |
|----------|---------------------|-----------------|---------------|------------|-------------|---------|------------------------|
| | | | | | 9 x 9 | 18 x 18 | |
| 128 | 3,909 | 4,427 | 38,790 | 19 | 2 | 3 | 149 |
| 512 | 3,976 | 4,512 | 137,384 | 35 | 2 | 3 | 146 |
| 1,024 | 3,834 | 4,461 | 271,780 | 57 | 2 | 3 | 140 |
| 2,048 | 4,015 | 4,566 | 535,950 | 77 | 2 | 3 | 144 |



More detailed information on the reference design can be found in *AN 412: A Scalable OFDMA Engine for Mobile WiMAX*: www.altera.com/literature/an/an412.pdf.

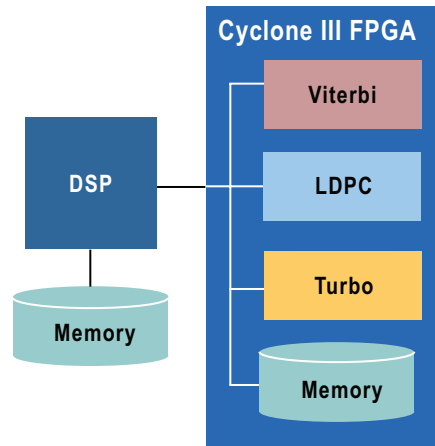
WiMAX Turbo Decoding

Forward error correction (FEC) decoding schemes—including Viterbi decoding, Turbo convolutional decoding, Turbo product decoding, and LDPC decoding—are computationally intensive and consume significant bandwidth when executed on software programmable multipliers. FPGAs are widely used to off-load these functions and free DSP bandwidth to perform other functions. These same FPGAs can also be used to interface to the MAC layer as well as accomplish certain lower MAC functions such as encryption/decryption and authentication. Altera's low-cost, memory-rich Cyclone III FPGAs are well suited to carry out such DSP coprocessing functionality, with the right mix

of logic-to-memory ratio. For example, WiMAX convolutional Turbo decoding at 20 Mbps can be implemented in less than 10 percent of the LEs and less than five percent of the memory in an EP3C55 FPGA.

Figure 5 illustrates how various FEC decoding schemes can be off-loaded from a multiplier to an FPGA coprocessor.

Figure 5. Using an FPGA Coprocessor for WiMAX Baseband Processing



Conclusion

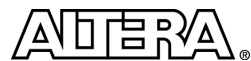
With up to 3.9M bits of RAM, 120,000 LEs, and 288 18 x 18 multipliers, Cyclone III FPGAs can integrate more end-application functionality than Cyclone II FPGAs, all at a lower cost and power. For example, the DUC and DDC, DL and UL OFDMA Engines, and CTC decoding functionalities in the WiMAX pico base station example can all be integrated in a midrange Cyclone III EP3C55 FPGA with less than 2 W of power consumption and a price of less than US\$29. In summary, with its unprecedented combination of power, functionality, and cost, the Cyclone III FPGA family enables a number of high-volume, cost-sensitive emerging wireless applications.

Further Information

- WiMAX Channel Card Solutions:
www.altera.com/end-markets/wireless/broadband/wimax/channel-card/wir-wimax-channel.html
- WiMAX RF Card Solutions:
www.altera.com/end-markets/wireless/broadband/wimax/rf-card/wir-wimax-rf.html
- FPGAs as Coprocessors for DSP Applications:
www.altera.com/technology/dsp/devices/fpga/dsp-fpga_coprocessor.html
- Altera's DSP IP Cores:
www.altera.com/products/ip/dsp/ipm-index.jsp
- Cyclone III End Market Applications:
www.altera.com/cyclone3-markets

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