
Using Cyclone III FPGAs for Clearer LCD HDTV Implementation

Introduction

Today's liquid crystal display (LCD) technology has found a great application with high-definition TV (HDTV), but the challenge has been to achieve high resolution, which requires faster data rates. Accelerating data rates require special image processing algorithms to support faster moving video. The industry is confronted with a major problem: how do you implement these algorithms and get a product out to market first, and do it within a known power budget?

To compound the problem, designers need to determine how to reconfigure the image-processing algorithms when the hardware platform connects to different sizes of LCD panels. Larger LCD panels require faster data rates, so the challenge is how to adjust the data rate for the panel size.

Those challenges are easily managed with the new low-cost Cyclone® III FPGA family. Designers can apply image-processing algorithms in Cyclone III FPGAs to convert and map digital video signals onto the display panel. In addition, designers can take advantage of the Cyclone III FPGA's flexibility to reconfigure image-processing algorithms to increase the data rate for larger display panels. Thus, designers can develop a common hardware platform for all of their LCD panels, no matter the size.

Benefits of Cyclone III FPGAs

Cyclone III FPGAs provide an effective blend of cost, performance, and flexibility for digital televisions and displays. Manufacturers of LCD TVs can use a Cyclone III FPGA as a coprocessor, running a real-time embedded operating system to control the complete display apparatus. Besides the central control of the display, designers can use Cyclone III FPGAs along with ASSPs in the data path for specific video and image processing. For example, FPGAs are ideal for optional display features, where they perform real-time image scaling on the video stream.

Cyclone III FPGAs include up to 288 optimized hard-coded digital signal processing (DSP) blocks, which form the basic elements of video and image processing. DSP blocks possess high-speed parallel processing capabilities ideal for executing DSP applications, such as image processing, that require high data throughput. The most commonly used DSP functions include finite impulse response (FIR) filters, complex FIR filters, fast Fourier transform (FFT), discrete cosine transform (DCT), and correlators. These functions are the building blocks for HDTV and other complex LCD applications.

New Technologies Overcome HDTV Obstacles

Today's larger displays can turn small artifacts into major image problems, defeating the very reason why a consumer purchases a larger display. Display designers must find a way to filter out those artifacts and smooth any jagged edges or jerky motion.

The options for implementing such image processing logic are to use ASSPs, ASICs, or FPGAs. Unfortunately for designers, ASSPs do not allow companies to differentiate their products, while ASIC development takes a long time and is very expensive. Only FPGAs offer the fast design and flexibility to complete a design fast and get it to market ahead of the competition. Now Cyclone III FPGAs deliver the lowest cost and power consumption than any other FPGA in the market today, offering two more reasons why FPGAs have become the preferred solution for image processing.

In addition, today's new HDTVs offer a great viewing experience, but often have to deal with the older standard-definition (SD) input. Display companies want to enhance the SD input image, and a scaling function, easily employed in a Cyclone III FPGA along with a core from the Altera® Video and Image Processing Suite, allows them to do so. [Table 1](#) lists the different MegaCore® functions available.

Table 1. Available IP MegaCore Functions

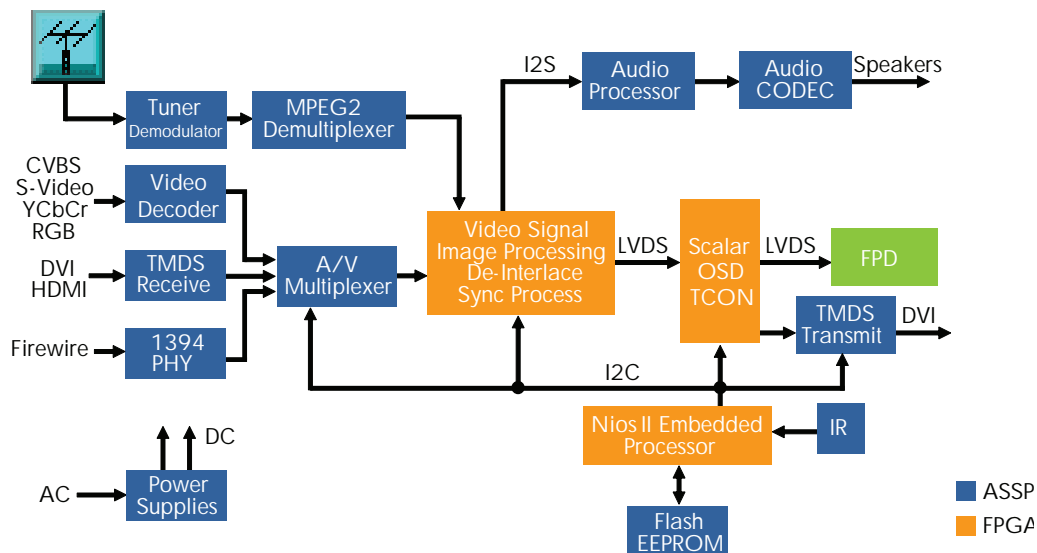
IP MegaCore Functions	Description
Color Space Converter	Converts image data between a variety of different color spaces
Chroma Resampler	Changes the sampling rate of the chroma data for image frames
Gamma Corrector	Performs gamma correction on a color space
2D FIR Filter	Implements a 3x3, 5x5, or 7x7 FIR filter on an image data stream to smooth or sharpen images
2D Median Filter	Implements a 3x3, 5x5, or 7x7 filter that removes noise in an image by replacing each pixel value with the median of neighboring pixel values
Alpha Blending Mixer	Mixes and blends multiple image streams
Scaler	Resizes and clips image frames
De-Interlacer	Converts interlaced video formats to progressive video format
Line Buffer Compiler	Efficiently maps image line buffers to Altera on-chip memory

Video Input Formats

In a typical digital LCD TV block (shown in Figure 1), the tuner module can be a satellite, terrestrial, or cable demodulator with either an MPEG2 or an MPEG4 decoder. Besides the signal from the digital TV tuner, a typical LCD TV also provides external video input such as DVI (Digital Visual Interface) or HDMI (High-Definition Multimedia Interface), analog RGB, CVBS, S-video, and component video.

The LCD HDTV monitor must be able to handle various video input formats. Some formats may directly be mapped into the display while others must be rescaled for proper viewing.

Figure 1. Typical Digital LCD TV Block Diagram



Nios Embedded Processors

Instead of using hard logic (often in the form of state machines) for control functions, designers are turning to Nios[®] II embedded processors for several reasons. First, they are often much easier to design and debug than HDL. Beyond the ease of development, designers prefer the versatility of a single CPU and toolset that fits a wide range of applications. Furthermore, a Nios II soft processor is a very cost-effective solution, as there is no need for an external processor and designers can embed it into the existing FPGA design with no additional cost.

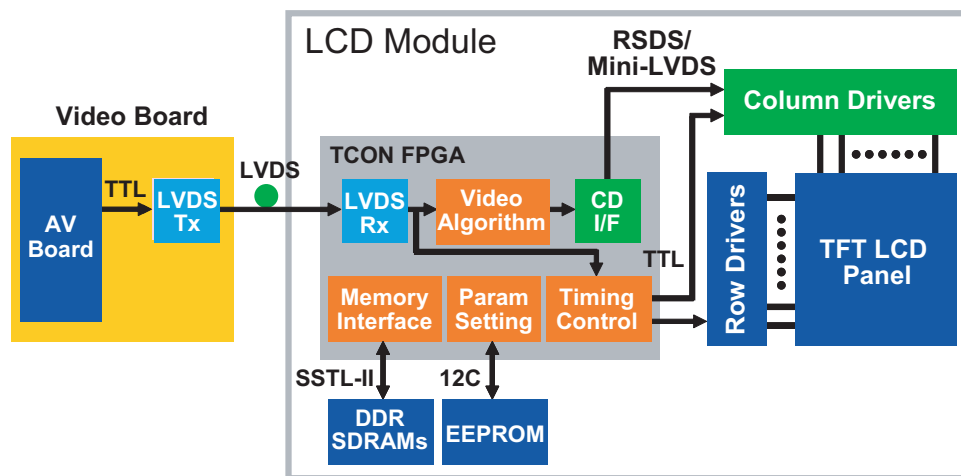
For DTV applications, Nios II processors control all data traffic, including:

- Routing video streams to the display
- Remote control handling
- General housekeeping activities
- Handling conditional access interface, such as smart cards
- Decrypting control words from the video stream

FPGA Advantages

The heart of the LCD HDTV is its image processing and timing control block (shown in Figure 2). The image-processing block typically includes functions such as scan rate converter, frame rate converter, color decoder, motion detection, scalar, and de-interlacing.

Figure 2. Typical LCD TV Interface Block Diagram



The color response time of an HDTV LCD display is slower than a conventional display, and depends on the color content. This challenges the development of image-processing algorithms when the additional requirement to eliminate any viewing artifact is factored in. Cyclone III FPGAs' design flexibility offers a significant advantage, allowing designers to redesign the algorithm within the device without having to reprogram it.

What is more important is that the Cyclone III family offers a wide range of capability, including density, on-board memory, and I/O, that designers can make use of in order to design the right application for their end product.

For example, the above design uses a single timing controller channel, and is intended for small or low-resolution displays. However, with Cyclone III FPGAs, designers can use a 2-channel timing controller and support higher resolution displays or much larger (greater than 36 inch) displays. The Cyclone III family offers features beyond any other low-cost FPGA to support these applications, including:

- Faster I/O for external memory access
 - X36 DDR2 up to 200 MHz
- Increased block size of memory to 9 Kbits for more efficient video line buffering
- Easier I/O design using integrated differential buffers with on-chip termination-including LVDS, mini-LVDS, and RSDS-to eliminate external resistors and simplify PCB layout
- Flexible PLLs offering:
 - More outputs, with up to 20 global clocks per device
 - On-the-fly dynamic PLL phase and frequency adjustment to support changing refresh rates
 - PLL cascading without routing off-chip to simplify PCB layout

- Support for input clock frequency down to 5 MHz to support low-cost clocks
- Low power, a significant advantage in these environments that are often significantly higher temperature compared to other consumer applications

I/O Flexibility

Cyclone III FPGAs also offer significant I/O flexibility, which is a major plus for engineers developing designs in an environment in which new standards are constantly emerging. For example, in the above design (Figure 2) the video board interfaces to the LCD module via an LVDS bus. In the future, standards such as DisplayPort, which is currently getting a great deal of attention in the market due to its ability to support both personal computers and home entertainment systems, could become the interface of choice. However, such new standards are not often supported by many ASSPs, and engineers will look to FPGAs to provide the required functionality with the right interface. Cyclone III FPGAs will support such standards with their ability to connect to a wide range of standards and the PLL outputs to deliver the necessary timing and control.

Another example of the value of the I/O available in Cyclone III FPGAs is RSDS, which was available on previous generations of Cyclone devices, but now also includes on-chip termination. Now designers can achieve higher signal integrity and reduce component count by removing the resistor packs often required for the interface.

Video Enhancement

Display manufacturers can complete their development fast and take advantage of a market opportunity by using Cyclone III FPGAs along with the Video and Imaging Processing Suite discussed above, while differentiating their products by adding proprietary algorithms for true color and motion performance. There are two methods of proprietary video enhancement used for creating a true video performance from an LCD panel.

The first, a technique called temporal dithering, generates a true gray scale for different colors by rapidly switching the pixels between on and off over a certain time period. The second, spatial dithering, generates the exact amount of color intensity scale. Spatial dithering can cause spatial noise, or error diffusion; further filtering and fine-tuning are required to correct this type of noise.

Performance

Cyclone III FPGAs offer a dramatic increase in performance because of the DSP processing capability offered, including up to 4 Mbits of RAM, up to 288 hard-coded DSP blocks, and up to 120K logic elements. Cyclone III FPGAs offer the capabilities often supported by several DSP processors, offering designers reduced cost, higher integration, and significantly lower power.

Conclusion

LCDs, originally designed for steady computer data text and graphics, now display fast-moving video content over much larger display panels. This capability requires special image processing algorithms that can be implemented with FPGAs. The Cyclone III family of FPGAs offers LCD designers the density and feature set to reconfigure these algorithms based on panel size within a standard hardware platform, which can help reduce manufacturing cost and speed time to market. In addition, designers can use the Cyclone III FPGA's flexibility for dynamic image processing to take LCDs even further into leading-edge commercial TV and display applications.

Acknowledgements

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