

Using Zero-Power CPLDs to Substantially Lower Power Consumption in Portable Applications

Introduction

Traditionally, the terms “low power” and “programmable logic” have not been used in the same context. However, the advent of the zero-power CPLD has transformed the discussion, as this technology brings the many advantages of programmable logic to designers of low-power electronic products. Now, in addition to the CPLD’s demonstrated ability to excel in general-purpose applications, zero-power CPLDs can reduce overall power consumption in portable products.

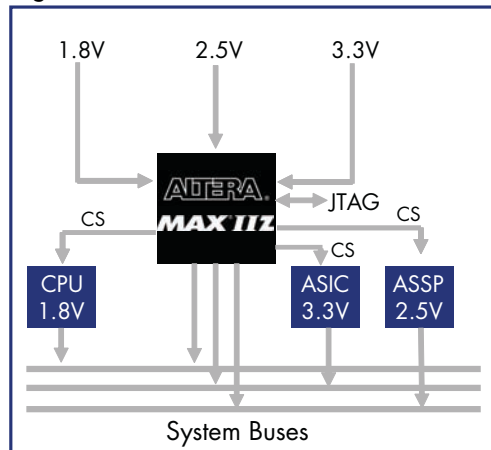
General-Purpose CPLD Applications

This first group of applications represents functions for which CPLDs excel. While these are not specific to reducing power, nevertheless, using a low-power CPLD to accomplish them has a positive net effect on power consumption. For example, a common CPLD function is to consolidate discrete logic. This saves space on the PCB, reduces bill of materials (BOM) costs, and lowers the overall power consumption. The next several sections discuss some common general-purpose CPLD applications.

Power Sequencing

In many products, the power-up order of the various devices is important, making power sequencing a critical function. A CPLD is live within microseconds of the system power-on, making it an excellent choice for controlling the power-up order of the various devices in the system, including a microprocessor or microcontroller (Figure 1). This power sequencing is just one of many system functions that the low-power CPLD can accomplish. Obtaining the highest value from programmable logic comes from incorporating several functions into one device.

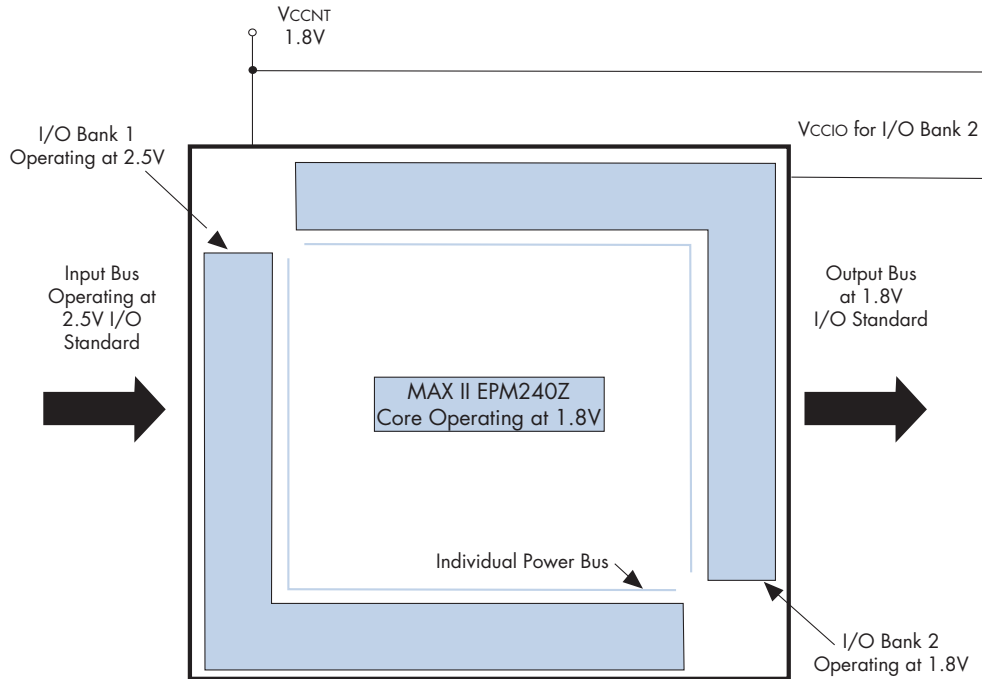
Figure 1. Power Sequencing Using a CPLD



Voltage-Level Translation

Many products require the use of logic devices of varying voltages. To support multi-voltage applications, designers frequently need to connect devices of differing voltage levels. CPLDs have a large number of I/Os, which are grouped into multiple banks. Each I/O bank is, in turn, assigned a unique voltage source. Thus, creating a voltage-level shifter is merely a matter of grouping all the I/Os of one voltage in one bank and connecting the associated voltage reference to the power rail needed for those I/Os (Figure 2). While it is useful to be able to accomplish level shifting using a CPLD, an even greater advantage is derived from the power of programmability combined with the level shifting. For example, if an application calls for a LCD display that is not supported by the host processor and is not at the same voltage level, a CPLD could be used to provide voltage-level shifted timing control between the host processor and a LCD display.

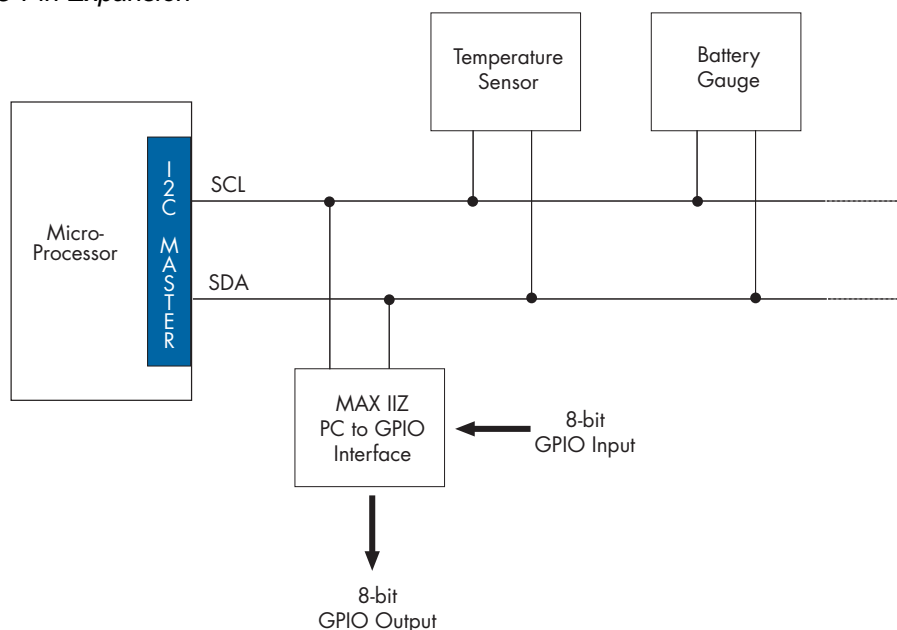
Figure 2. Using an Altera MAX IIZ CPLD to Perform Voltage-Level Shifting



General-Purpose I/O Pin Expansion

There are many cases where the CPLD makes an excellent companion to a microcontroller, ASSP, or ASIC. For example, in a common application known as general-purpose I/O (GPIO) pin expansion, designers combine the programming capabilities of a small, inexpensive microcontroller with the GPIO resources of a CPLD. The CPLD builds a set of internal registers that can be accessed by the microcontroller through any available serial port such as I²C or SPI (Figure 3), allowing the microcontroller to use its existing serial port to expand its total I/O count. CPLD-expanded I/Os can also be used to accomplish voltage level shifting, thus increasing the utility of the CPLD.(1)

Figure 3. GPIO Pin Expansion



While the example given uses a microcontroller, it is equally applicable to an ASSP or ASIC. For example, many designers have discovered that a small ASIC driving a CPLD through a serial interface is a more inexpensive solution than producing one large ASIC with the same I/O capabilities.

Interface Bridging

Portable application designers often find a need to connect devices with differing I/O interfaces. This function is referred to as bridging because the CPLD is used to form a bridge between the dissimilar interfaces. Figure 4 illustrates the use of a CPLD to bridge between two differing serial interfaces: I²C and SPI. This design can be employed in an Altera® MAX® IIZ EPM240Z CPLD, using about 43 percent of the available logic and six I/O pins.(2)

Figure 4. I²C-to-SPI Interface Using a MAX IIZ CPLD

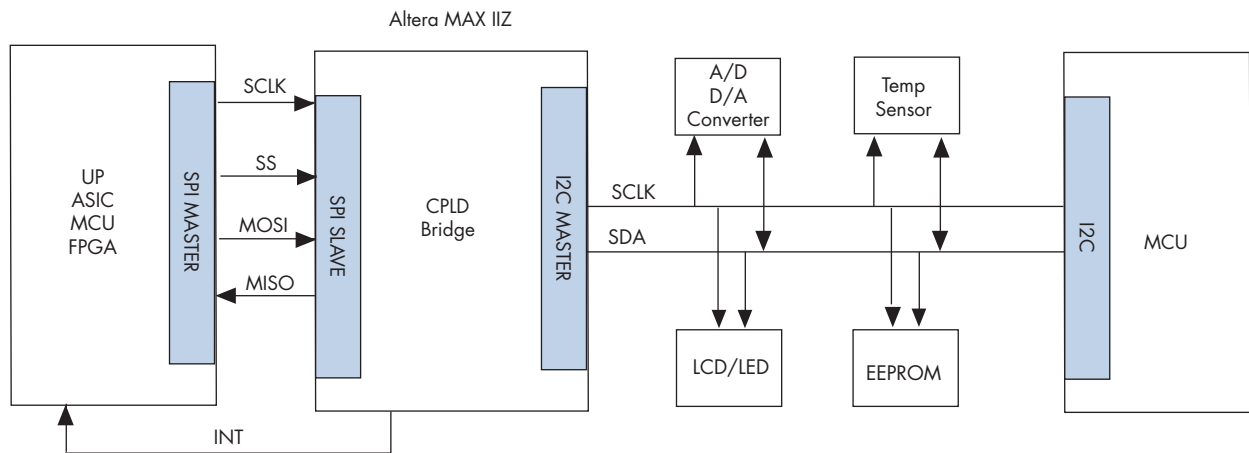
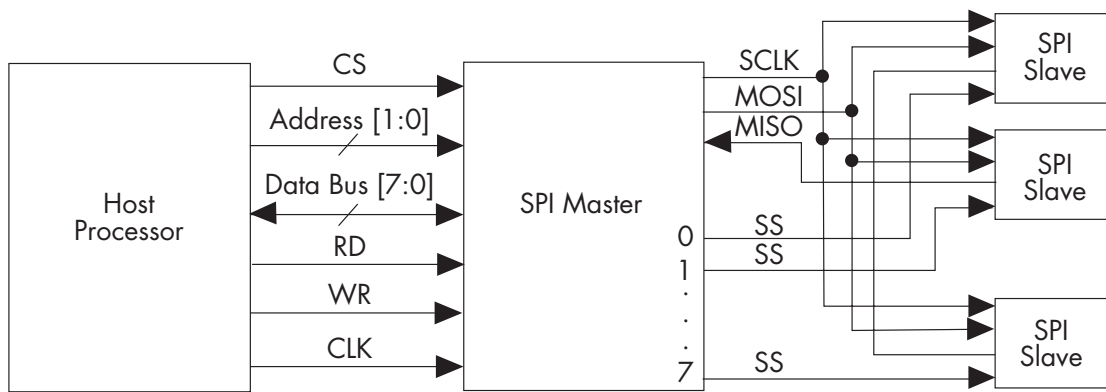


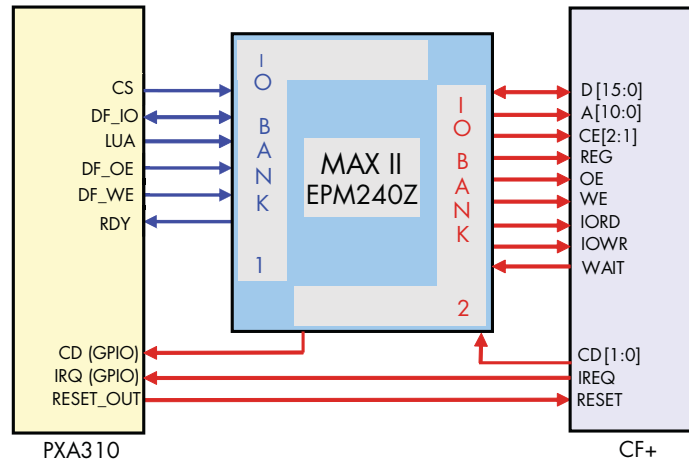
Figure 5 shows a host processor interfaced to a SPI master as an example of using a CPLD to implement a serial-to-parallel interface. This example creates a host-processor bus interface and a complete SPI master, and can be implemented in a MAX IIZ EPM240Z CPLD, using about 30 percent of the available logic and 25 I/O pins.(3)

Figure 5. Host Processor-to-SPI Interface Using a MAX IIZ CPLD



In Figure 6, a CPLD is used to bridge between two different parallel interfaces. This design example implements a PXA310 host-processor bus interface to a Compact FLASH+ device. It can be implemented in a MAX IIZ EPM240Z CPLD, using about 17 percent of the available logic and 59 I/O pins.(4)

Figure 6. Host Processor-to-CF+ Interface Using a MAX IIZ CPLD



Applications for Reducing Power Consumption

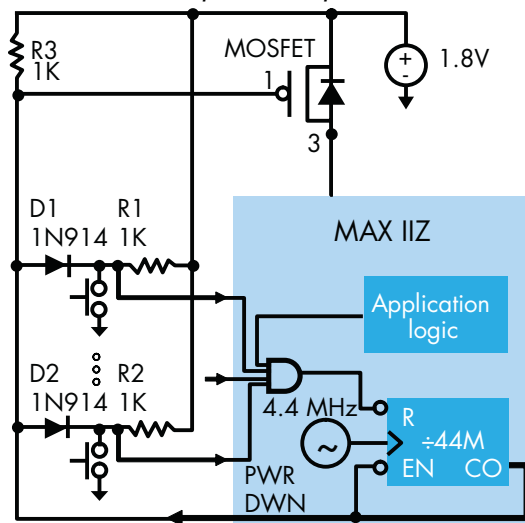
The previous applications discussed demonstrate the use of a low-power CPLD to accomplish many of the functions common to portable applications. The next group of applications illustrates specific ways to use the unique features of a zero-power CPLD to reduce the power consumption in portable applications.

Self Power-Down and Power-Up

The MAX IIZ CPLD provides an example of a zero-power CPLD with ultra-low standby power consumption. An EPM240Z device, for instance, consumes just 29 μA in standby. However, in order to achieve the absolute lowest power, it would be ideal if a device consumed no power when it was not being used. Surprisingly, this is actually achievable because, unlike traditional macrocell-based CPLDs, the MAX IIZ device contains an internal oscillator that can be used to build an auto-power-down capability.

The operation is simple; all of the inputs to the MAX IIZ CPLD are used to control a counter. If any input is active, the counter is held on reset. When all of the inputs go inactive, the counter counts until a user-defined length of time has passed. If during this time all of the inputs are still inactive, a signal is sent to disable a metal-oxide-semiconductor field-effect transistor (MOSFET), which shuts off power to the MAX IIZ device. When any input goes active again, the internal counter is reset, power is applied, and the MAX IIZ CPLD powers up (Figure 7).

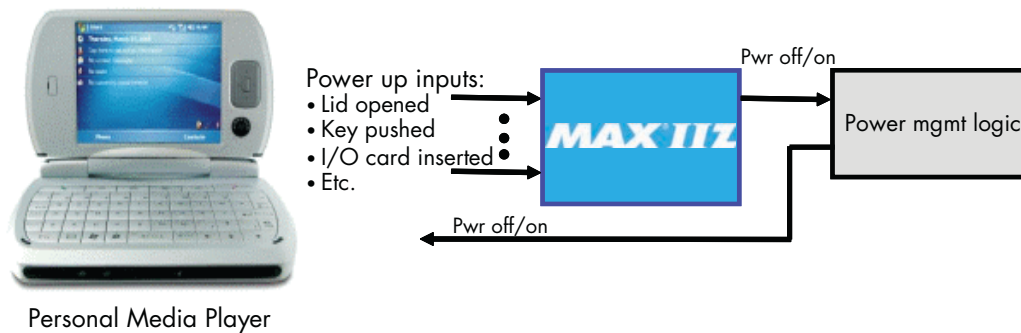
Figure 7. Auto-Power-Down and Auto-Power-Up When Inputs Are Inactive



Powering Up With Multiple Input Possibilities

The ability of the MAX IIZ CPLD to easily monitor its inputs and do a self-stop or self-start has direct application to power consumption reduction in portable applications. In many portable products, power-up is accomplished by the push of a power-up button. If the product is idle for some period of time, a shutdown or standby mode is invoked to conserve battery life. At this point, many portable designers would like any user action to re-activate the product—for example, opening the cover, pushing any key, inserting a memory card, etc. (Figure 8). However, many power management designs only allow one control input. In this case, the CPLD can be used to monitor the inputs. When the product is idle for a designer-determined period of time, the CPLD issues a power-off signal to the power management logic. Then when any input goes active, the CPLD powers up and issues a system power-up signal to the power management logic.

Figure 8. Using a MAX IIZ CPLD to Start and Stop System Power Based on Input Activity

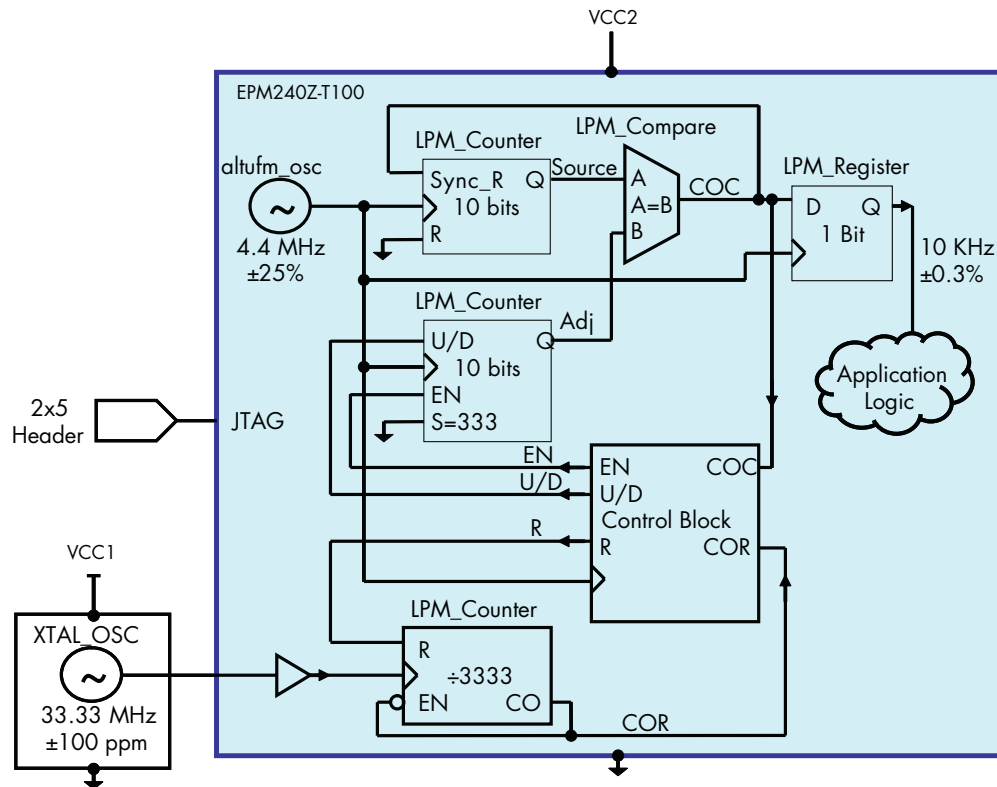


Using a CPLD as a Power-Reducing Coprocessor

There are many system functions that can be off-loaded from a large, power-hungry host system processor to a small power-frugal CPLD. One group consists of the many system “housekeeping” functions that must be done on a periodic basis. In the following examples, the system processor can remain in a power-savings mode, while the low-power MAX IIZ CPLD uses its internal oscillator to periodically execute the task. If desired, the internal oscillator of the MAX IIZ CPLD can be calibrated to an external oscillator. After calibration, the external oscillator can be powered off, for even more power savings (Figure 9).

- *Monitoring the system status:* Periodically, the CPLD checks the system status. If all is well, it powers back off, but if there is a problem, the CPLD logs the problem and wakes the host processor.
- *Blinking a Bluetooth LED:* Common to many portable applications, blinking a Bluetooth LED is a natural application for a CPLD. The alternative, waking the host processor and enough of the rest of the system to do this, consumes far more power than using just a CPLD.
- *Monitoring a battery gauge:* While the host processor remains in standby, the CPLD periodically reads the battery gauge. If power falls below a specified level, the CPLD wakes the host processor and a graceful shutdown ensues.

Figure 9. Calibrating the CPLD's Internal Oscillator to an External Source



Using a CPLD to build a low power media coprocessor provides another opportunity for significant power savings. In this application, instead of having the host processor stream the media file to a CODEC, the host processor is put to sleep and the CPLD is used. Typically, the power consumption of a CPLD doing this function is in the low microamps, compared to the milliamps required by the host processor. This power savings directly translates in longer battery life.

Summary

Traditionally, low-power portable product designers have not been able to take advantage of the many benefits that programmable logic has to offer. However, zero-power CPLDs with standby current in the low micro-amps now make these programmable devices a viable option for low-power product designers.

Showing examples of using CPLDs to implement general-purpose system functions, this paper illustrates the unique ability to build self-stopping and self-starting circuits in MAX IIZ CPLDs. This capability is then applied to show specific applications for reducing power consumption in portable applications. In addition, this paper shows how to offload tasks such as periodic system monitoring and media streaming, from the host processor to a lower power CPLD coprocessor. As a result of zero-power CPLDs, portable electronics product designers now have an even greater ability to create innovative, low-power, feature-rich products.

References

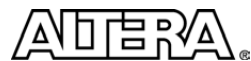
1. *AN 494: GPIO Pin Expansion Using I²C Bust Interface in an Altera MAX II CPLD:*
www.altera.com/literature/an/an494.pdf
2. *AN: 486: SPI to I²C Using MAX II CPLDs:*
www.altera.com/literature/an/an486.pdf
3. *AN 485: Serial Peripheral Interface (SPI) Master in Altera MAX II CPLDs:*
www.altera.com/literature/an/an485.pdf
4. *Design Example 200: CF+ Interface for the PXA310 Using MAX II CPLDs*
www.altera.com/literature/an/an492_design_example.zip
5. *AN 491: Auto Start Using Altera MAX II CPLDs:*
www.altera.com/literature/an/an491.pdf

Further Information

- Download design examples:
www.altera.com/support/examples/max/exm-max.html
- *Reduce Total System Cost in Portable Applications Using MAX II CPLDs:*
www.altera.com/literature/wp/wp-01001-reduce-total-system-cost-in-portable-apps-using-max.pdf
- *Six Ways to Replace a Microcontroller With a CPLD:*
www.altera.com/literature/wp/wp-01041-six-ways-to-replace-microcontroller-with-cpld.pdf
- *AN 422: Power Management in Portable Systems Using MAX II CPLDs:*
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- Download free Quartus® II Web Edition Design Software:
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www.altera.com/products/devkits/altera/kit-maxii-1270.html
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Acknowledgements

- Rafael Camarota, Senior Manager, HardCopy® Product Group, Altera Corporation
- Denny Steele, Senior Manager, Low-Cost Products Group, Altera Corporation



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