

## Supporting Digital Television Trends with Next-Generation FPGAs

**Question:** What do the following items have in common?

- iPhones
- Avatar 3D (James Cameron's new movie)
- Digital SLR cameras
- LCD digital televisions

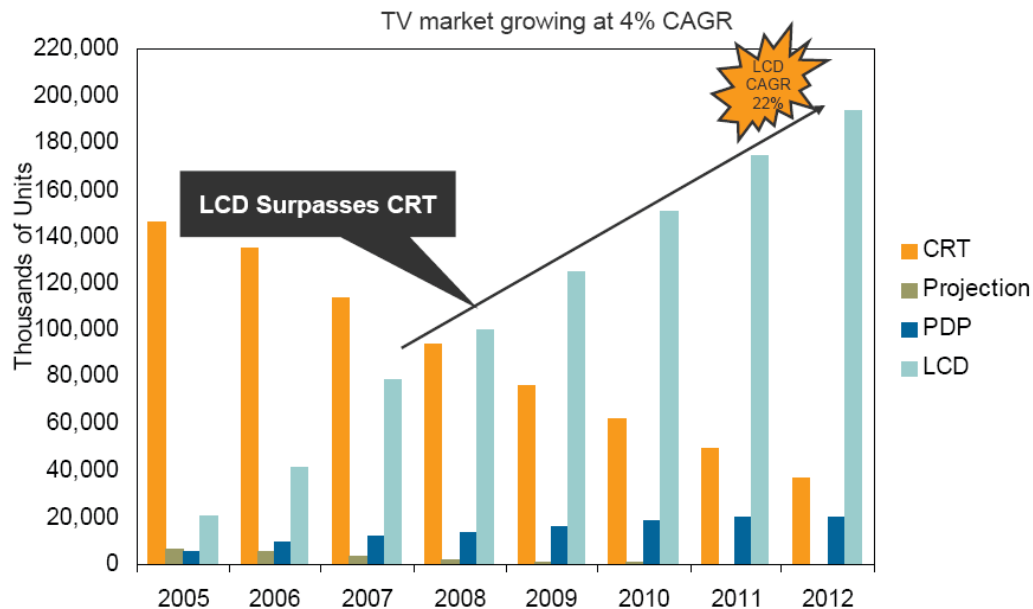
**Answer:** They are all evidence that consumers strongly prefer products with “stunning” visuals.

This white paper shows how these trends towards new features and faster introduction rates of new models are fueling increased FPGA use within high-definition television electronics.

### Introduction

The digital television market is growing, with the number of liquid crystal display (LCD)-based digital televisions growing at 22% CAGR (Figure 1). More recent forecasts show growth in 2010 of 6% over 2009's 1% decline(1).

Figure 1. LCD Digital Television Growth Rate



Source: iSupply Corporation *Television Systems Market Tracker*(2)

### Traditional Digital Television Functions

The digital logic requirements imposed by LCD, plasma display panel (PDP), and projection televisions are very similar. These requirements are video processing and high bandwidth chip-to-chip communication. Altera has developed and currently supports solutions for this functionality.

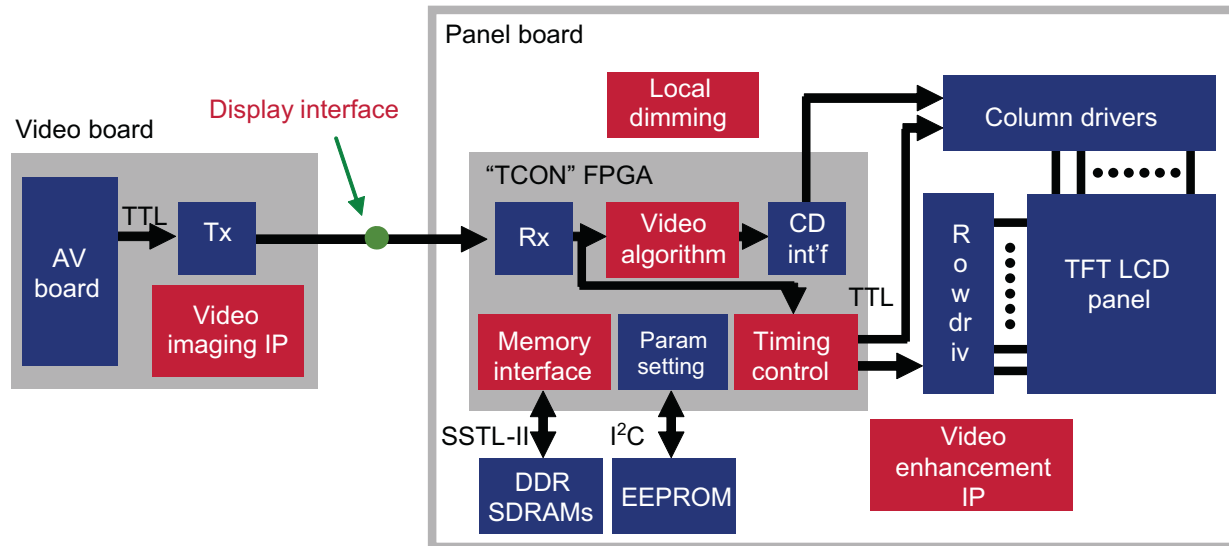
Traditional functions that digital television manufacturers have designed using Altera® Cyclone® FPGAs include:

- Timing controller (TCON), using proprietary customer algorithms
- Video intellectual property (IP), such as temporal or spatial dithering

- Picture quality enhancement, such as frame rate conversion and local dimming for LED back-light units
- Display interface, including next-generation protocols like V-by-One and DisplayPort

Figure 2 illustrates how these sub-functions are interrelated.

Figure 2. FPGA Implementation of TCON Function



## Next-Generation Digital Television Functions

The big question for digital television is, “What is the next break-out technology?” According to Display Search, advanced technologies like LED backlights, 3D, and higher frame rates (i.e., greater than 120 MHz) will be driving explosive growth for LCD televisions over the next few years. Other factors coming into play are the on-going economic pressure to lower costs and the “green” movement towards lower power.

Altera’s Cyclone series FPGAs are well suited for quickly implementing these traditional functions. Other semiconductor vendors may argue they can quickly implement these functions into new ASSPs or system-on-chip (SoC) ASICs. Digital televisions are high-volume and cost-sensitive products, but the life-cycle for each model is very short-lived. Digital television OEMs are always incorporating new features to address market trends, and today’s set of next-generation features are no exception, making it hard to justify the return on investment for creating a new ASSP or SoC ASIC.

Next-generation DTV features include:

- Better resolution (i.e., 1080p to 4k2k)
- 3D
- LED backlighting
- Bigger screen sizes
- Higher frame rates (i.e., 120 MHz to 240 MHz)
- Lower costs
- Lower power consumption

## Digital Television Design Challenges

How can the OEMs incorporate these new features while simultaneously tackling the everyday technical and business challenges for designing new electronic subsystems? Some of these challenges are:

- Technical
  - Current display interfaces connecting subsystems running out of bandwidth (i.e., LVDS)
  - Choosing the best architecture for internal/external video connection; HDMI, DVI or other
  - Higher frame rates + higher resolution = faster data rates, requiring more video processing power and higher bandwidth to transfer data between subsystems
  - Lowering power
- Business
  - Product differentiation versus competitors
  - Engineers learning new technologies and architectures
  - Lowering cost
  - Shorter life-cycle per model
  - Shorter development cycle
- New technologies
  - V-by-1, DisplayPort, Embedded DisplayPort, etc.
  - Next-generation FPGA features

Use of FPGAs is increasing because they provide the most flexibility, faster time-to-market, and low-enough cost structure (compared to ASSP and SoC ASICs), all of which allow OEMs to sell new models with higher ASPs with new features and increased functionality.

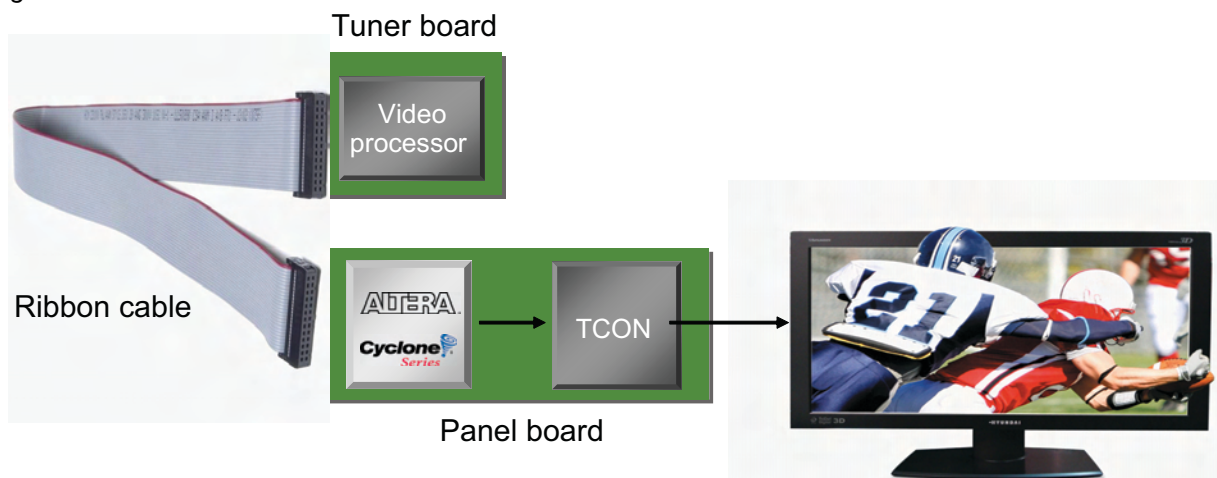
## Board Interface Example

To illustrate the value of FPGAs more concretely, let us look in more detail at one technical challenge and one new feature.

### *Bandwidth Bottleneck*

A majority of the video processing within a digital television is done on the video board subsystem. As more processing is required to handle new features and functions, more bandwidth is required to transfer this information to the panel board. Mainstream digital televisions use LVDS as an interface between the two boards (Figure 3).

Figure 3. Board Interface Bandwidth Bottleneck



The number of LVDS I/Os can be increased to handle higher bandwidths but comes with higher cost structure: a larger LVDS connector on both boards, a wider ribbon cable between the connectors, and more high-speed traces required on both video and panel PCB. Table 1 summarizes and compares the two interface options, along with a base line (single-ended I/Os), for implementing a higher bandwidth board-to-board interface.

Table 1. Interface Options for Video to Panel Board

Interface Options	Example I/O Standard	Maximum Performance	Clock Architecture	Comparison (1080p, 120 MHz, 10 bits per color)
Single-ended I/Os	LVC MOS	~400 MHz	Separate from I/Os	N/A
Differential I/Os	LVDS	~1,200 MHz	Separate from I/Os	24 LVDS I/O pairs at 600 MHz + CLK
Transceiver I/Os	CDR	12,000 MHz	Embedded	4 DisplayPort transceiver I/Os at 2.7 Gbps

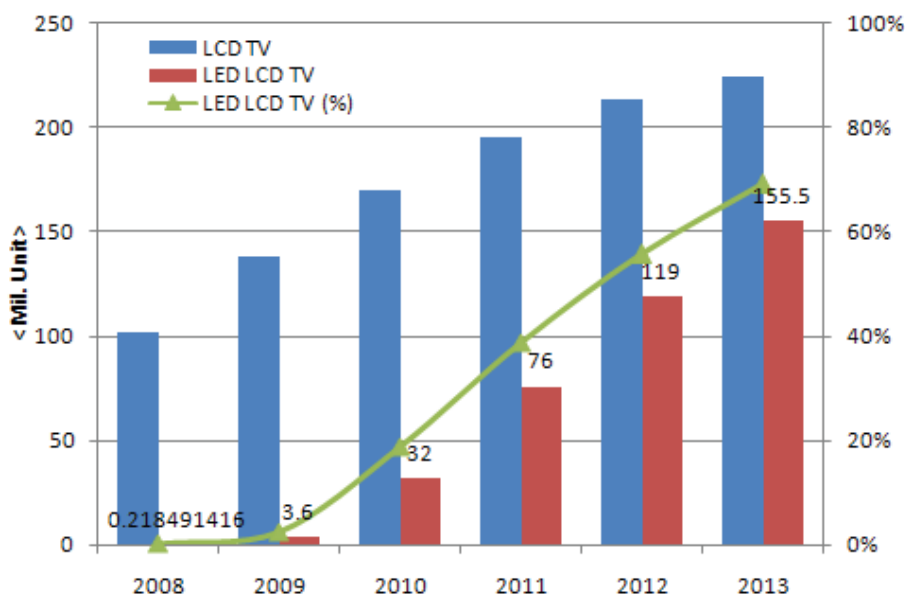
Clearly, the transceiver I/Os can support higher bandwidths. With the adoption of new transceiver-based video-centric protocols like high-speed LVDS, V-by-One and DisplayPort, the bottleneck between the video and panel boards not only will be eliminated but also provide a clear path to support higher bandwidths in the future. In addition, switching from LVDS to transceiver I/Os helps to decrease the cost structure, as well as the following benefits:

- Smaller, cheaper connectors and cable (25 I/Os to 4 I/Os)
- Fewer board traces resulting in less board area used, lowering the cost of PCBs
- Reduced data skew by using embedded clocks
- Lower EMI
- Lower power

### LED Backlight

The LED backlight is a new feature for dramatically improving picture clarity. Consumers are just now seeing examples (at CES 2010, Best Buy, etc.), which are dramatically driving up the forecast for this feature (Figure 4).

Figure 4. LED LCD TV Forecast

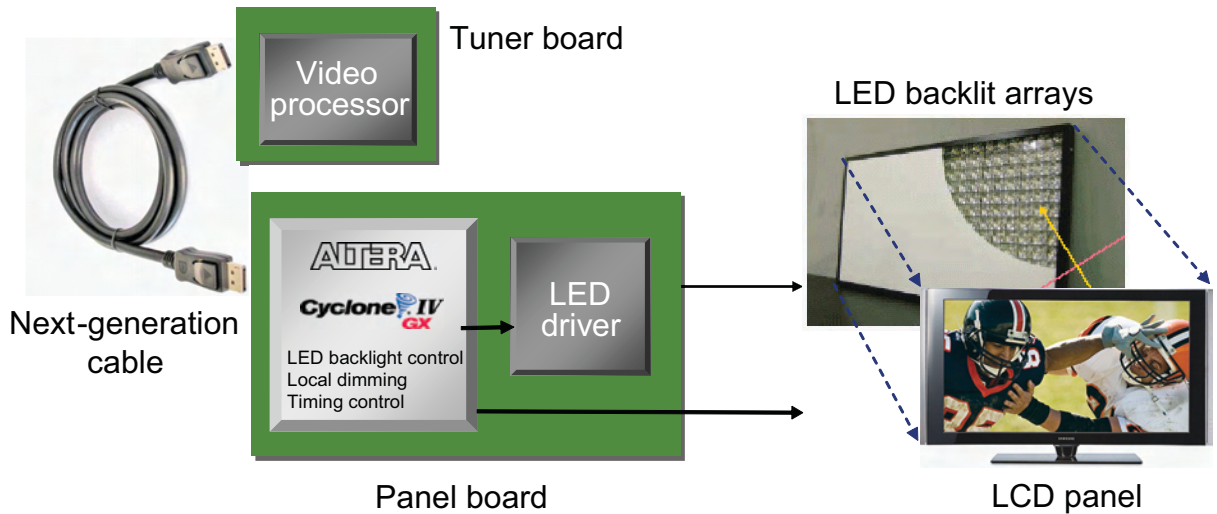


Source: LED LCD TV Makers Roadmap & Market Forecast, Displaybank, December 2009(3)

Currently, there is no standard for controlling backlight LEDs. Therefore, the control algorithms are different for each supplier (i.e., Samsung vs. Vizio), different for each digital television size (40" vs. 52"), and will continue to change as LED costs enable more LEDs per section to be added (Figure 5). Incorporating LED backlight functionality into an existing digital television ASIC or ASSP does not make business sense because of the changing and fragmented

requirements, which leaves FPGAs to fill the gap. Altera's Cyclone IV GX FPGAs can easily implement the transceiver I/Os needed to eliminate the display-interface bottleneck and provide video coprocessing for LED backlighting, working alongside existing video-processor ASSPs or ASICs.

Figure 5. LED Backlight Basics



Another HDTV function that can be implemented with FPGAs, but is not included in the scope of this paper, is noise reduction.

## Altera Solutions

Altera and its partners provide a robust set of building blocks for digital television OEMs, including:

- Cyclone IV FPGAs with embedded DSP capability, embedded soft IP 32-bit controllers, and high-speed transceiver I/Os
- Video and image processing IP
- Interface IP
- High-speed memory controller IP
- Reference designs

Altera's Video and Image Processing Suite (IPS-VIDEO) is an IP bundle consisting of nine functions with parameters that can be statically, or in some cases, dynamically changed. [Table 2](#) summarizes these functions.

Table 2. Functions Available With the Video and Image Processing Suite

Function	Description
2D FIR Filter	Implements 3x3, 5x5, or 7x7 finite impulse response (FIR) filter operation on an image data stream to smooth or sharpen images
2D Median Filter	Implements a 3x3, 5x5, or 7x7 filter that removes noise in an image by replacing each pixel value with the median of neighboring pixel values
Alpha Blending Mixer	Mixes and blends multiple image streams—useful for implementing text overlay and picture-in-picture mixing.
Chroma Resampler	Changes the sampling rate of the chroma data for image frames, for example from 4:2:2 to 4:4:4 or 4:2:2 to 4:2:0.
Clipper	Provides a way to clip video streams and can be configured at compile time or at run time.
Clocked Video Input/Output	These two cores convert the industry-standard clocked video format (BT-656) to Avalon® streaming (Avalon-ST) video and vice versa.
Color Plane Sequencer	Changes how color plane samples are transmitted across the Avalon-ST interface. This function can be used to split and join video streams, giving control over the routing of color plane samples.
Color Space Converter	Converts image data between a variety of different color spaces, such as RGB to YCrCb
Control Synchronizer	Synchronizes the changes made to the video stream in real time between two functions
Deinterlacer	Converts interlaced video formats to progressive video format using a motion adaptive deinterlacing algorithm. Also supports “bob” and “weave” algorithms
Frame Buffer	Buffers video frames into external RAM. This core supports double or triple-buffering with a range of options for frame dropping and repeating.
Frame Reader	Reads video from external memory and outputs it as a stream
Gamma Corrector	Performs gamma correction on a color plane/space
Scaler	A sophisticated polyphase scaler that allows custom scaling and real-time updates of both the image sizes and the scaling coefficients.
Switch	Allows video streams to be switched in real time
Test Pattern Generator	Generates a video stream that contains still color bars for use as a test pattern.

Altera and its partners also provide interface cores that are often required in a video system. Table 3 shows a partial listing of these types of cores and reference designs.

Table 3. Video Interfaces and System IP

Function	Company
10/100/1000 Ethernet	Altera, MorethanIP
32-bit RISC Processor <ul style="list-style-type: none"> <li>• Nios® II</li> <li>• ARM Cortex M1</li> <li>• V1 Coldfire</li> </ul>	Altera, ARM, Freescale
3D Rendering	DDD
ASI	Altera
Compact Flash and SD Interfaces	Altera
DDR/DDR2 Memory Controllers	Altera, Northwest Logic, Microtronix, CAST
Image Enhancement IP	Apical
Mobile DDR Memory Controllers	Northwest Logic, Microtronix
NOR Flash	Altera
SDI, 3G-SDI, Triple-Rate SDI, HD-SDI	Altera
SRIO Interface to External Processors	Altera
Video Over IP	Altera Reference Design

In addition, Altera offers various development kits, daughter cards, and demonstration boards, including ones using HDMI, DVI, V-by-One, and DisplayPort.

## Conclusion

The proliferation of so many different digital television models—better known as market fragmentation—and differing regional market requirements, combined with the desire to add new features and functions to respond to rapidly changing consumer demand is why FPGA-based digital television solutions are forecasted to grow in market share. Faster introduction rates of new models are also fueling increased use of FPGA. No matter what technology standards are adopted (or become de facto standards), they all share one common characteristic: their technology and business models are best solved by Altera FPGA-based solutions.

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## Further Information

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[www.altera.com/end-markets/consumer/dtv/csm-digitaltv.html](http://www.altera.com/end-markets/consumer/dtv/csm-digitaltv.html)
- Displays and Projectors System Usage:  
[www.altera.com/end-markets/consumer/projectors/csm-displays-proj.html](http://www.altera.com/end-markets/consumer/projectors/csm-displays-proj.html)
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- *Using Cyclone III FPGAs for Clearer LCD HDTV Implementation:*  
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