

# Selecting the Correct High Speed Transceiver Solution

## Introduction

Many standards and protocols are now using high speed transceivers (SERDES) as part of their physical interface. The protocols cover a spectrum of applications including communications, computer, industrial and storage, where there is a need to move large quantities of data between chips or across backplanes, but traditional parallel bus interfaces can no longer be relied upon. One technology emerging to support many of these applications is the FPGA architecture with embedded High Speed 3.125 Gbps transceivers. This allows the user to develop a full system of chip solutions by providing both a physical layer implementation and the logic to provide full hardware support for the rest of the application. These devices also provide all of the historical benefits of FPGA architecture including flexibility, ease of use and quick time to market, all qualities required as these new protocols emerge.

A number of solutions now exist in the market, including Application Specific Standard Product (ASSP), Application Specific Integrated Circuits (ASIC) and FPGA with Embedded high speed transceivers. This paper outlines some of the considerations when selecting among these products.

## ASSP for high speed design

Traditionally High Speed Interfacing has been implemented using ASSP devices. ASSP solutions tend to require multiple chips to provide the solution. This is partly due to the rate at which the technology grew, and partly because the transceiver requires different process technology compared to the rest of the system. Initially the system is very modular; for example, a SERDES solution would consist of a separate transceiver, a Serializer/Deserializer and an encoder/decoder. However more recently these have been merged into a single chip solution.

While it is common to integrate transceivers into higher layer IC's, the challenge remains for many ASSP vendors to define and design a chip that can support multiple protocols or applications. This is a challenging task since in most cases standards and market dynamics are in a constant state of flux. Today, some separation is still necessary because it is not possible to generate a "one fits all" protocol ASSP product, so it is often more cost effective to make a generic product which covers a number of applications. ASSP's reliance on multiple devices to provide a solution has a number of disadvantages to the high speed designer

- **Interoperability** Connectivity between ASSP's is generally parallelized for chip to chip transfer. In order to maintain the data rate, parallel interfaces must continue to run at (relatively) high speeds, support double data rates (data on both edges of the clock) and support wide bus widths. High speed parallel busses are extremely susceptible to skew between signal, noise and crosstalk, causing difficult layout conditions. These issues are greatly reduced by single chip solutions much of the data processing can occur in the same device as the transceiver, reducing the number of chip to chip connections. A good transceiver based solution will also provide a balanced parallel interface with additional circuitry to overcome skew and signal integrity issues.

- **Power** Multiple ASSP solutions have a greater power budget than a single chip solution. Firstly there is the issue of each device requiring its own core supply and secondly the parallel bus interfaces between ASSP's require additional power to be able to drive signals between chips. Both these issues can be significantly reduced by a single chip solution.
- **PCB layout** Multiple chip solutions require a more a complex layout. Firstly there is the issue of PCB real estate, where a single chip will require less room than multiple chip solutions, particularly when considering passives required for decoupling and signal integrity. Secondly, layout is complicated by the high speed, wide parallel (source synchronous busses) which must be carefully laid to avoid skew, noise and crosstalk.

ASSP's on the whole can provide a reasonable solution, particularly where the channel requirement is low. They are also ideal at the higher end of the market, where they can use dedicated processes to generate devices to reach higher data rates and better jitter requirements. However, many applications require the ASSP to interface to either an ASIC or FPGA for data processing, so as mainstream ASIC or FPGA embraces the transceiver architecture, it makes sense for engineers to use these solutions to overcome the issues highlighted above.

## ASIC for high speed design

ASIC has generally been viewed as a good single chip solution for high speed design. ASIC allows the user to fully customize the design to meet their application needs, overcoming issues such as channel limitations and it enables the user to add functionality around the transceiver for a particular application or protocol. ASIC enables the user to develop a full data path solution in a single chip, reducing the number of external busses between devices and removing some of the interoperability issues associated with interconnectivity.

However there are a number of new trends emerging which will make only the highest volume solutions viable for ASIC design.

- **Cost and Time** The cost and time to market issues of ASIC issues are heavily documented, particularly the design costs and design/verification time needed for low geometry process technologies such as a 0.13um all layer copper technology. Transceiver integrated ASIC devices require leading edge technology to enable the transceivers to operate at high speed. Therefore the ASIC designer has little alternative but to accept high NRE's charges and long development and high verification times if they are to implement design in ASIC.  
Embedding transceivers into a digital domain is complex and often causes significant design issues, particularly when preventing noise and jitter from crossing between the transceiver and the logic domains. It is also difficult to select the correct transceiver characteristics to meet the environment in which the device is likely to be used. These issues invariably lead to multiple iterations of the silicon, massively increasing the development costs. Modeling software is now available to overcome some these issues, but it is extremely expensive, time consuming and requires leading edge hardware to run and operate successfully.

- **Flexibility** Many new protocols are now adopting high speed transceiver technology as a standard interface technology. Many of the protocols are still standardizing so it is possible that some may merge or disappear. It is therefore important that the device technology used to support new protocols is flexible enough to cope with design issues or changes in order to extend the life of a product. ASIC is traditionally inflexible and often needs to go through a difficult redesign process to cope with a modification.

### *FPGA for high speed design*

The integration of transceivers with FPGA architectures provides the user with many of the benefits of the ASIC solution, but with the flexibility required to overcome changes in protocols or modifications required in design. The FPGA solution provides a single chip solution and therefore overcome many of the interoperability, layout and power requirements of multiple chip solutions. The transceivers supplied with FPGA are also flexible, allowing them to operate in a number of different system environments helping to overcome signal integrity issues. This flexible approach allows the same card to be used in a number of different systems and applications.

The transceiver within the FPGA architecture can be viewed as partial ASSP's. Engineering effort provided by the FPGA manufacturer reduces the effort required to design and verify the data path between the FPGA and the transceiver. The transceiver are also designed and tested to work to a specific criteria and to support specific protocols. These steps reduce the designer's characterization and test workload, during the compliance phase of the development and further reduce the time to market beyond the traditional advantages offered by FPGA's.

In applications where the data rate exceeds the FPGA transceiver speed, or protocols where the data throughput is higher than the bandwidth of FPGA, then it is possible that an ASSP or even an ASIC will provide a better solution. However in these applications transceiver based FPGA's will still play a part in the overall system design, and will interoperate with the other components in the system to provide a complete solution.

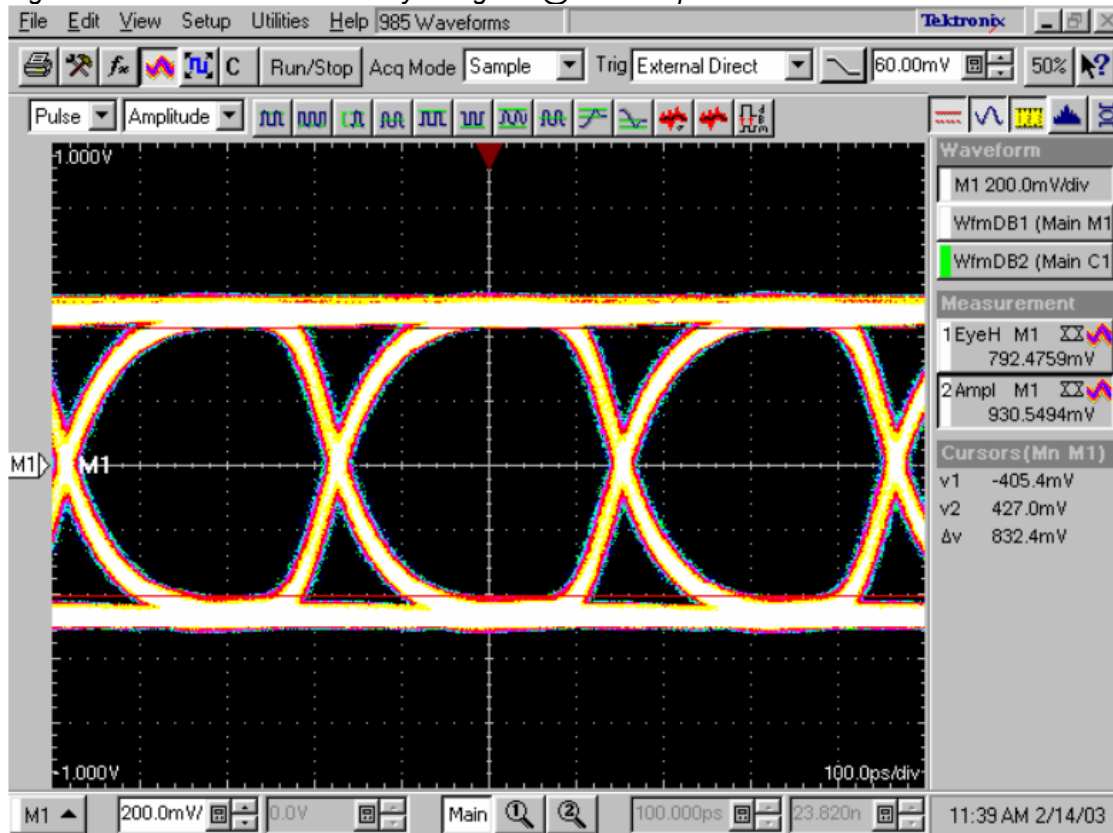
## **Considerations when choosing a transceiver**

Transceiver selection is fundamental to the whole system design, so decisions are made on performance rather than brand loyalty or the type of design tool used on the previous design. The selection can be as important as which Processor or DSP is to be used in the system, so the selection process often starts early in the design phase and is carried out with a great deal of care.

Generally, system architects analyze the performance of the transceiver before making final decisions. There are many criteria for the transceiver to meet during this selection phase, but the compliance to the specification and its immunity to adverse conditions such as susceptibility to jitter and noise, or its ability to drive along the transmission medium are key.

The empirical measurement of the transceiver performance is the eye diagram. This is a measurement of the transceiver waveform pattern built up over a number of cycles and superimposed.

Figure 1. Stratix GX transceiver eye diagram @ 3.125Gbps



The eye pattern can be used to show conformance to a particular specification by the use of an eye mask. If the waveform does not cross the mask then it is seen to conform to the specification for jitter, noise and amplitude. If the eye crosses the mask then it does not conform.

The Transceivers in the Stratix GX architecture are seen to have a superior eye quality. Figure 1 shows a 3.125Gbps eye diagram with 0% pre-emphasis and a VOD of 1000mV

While the transceiver performance is extremely important to the decision making process, there are also a number of other considerations which need to be made when selecting the correct device. The following section discusses some of these features.

## Power

Power consumption is one major issue in virtually all applications, but particularly in a chassis based systems, is power consumption. The fast switching requirements of the transceiver makes them inherently power hungry, leading to a high power requirement. Power issues are prevalent in all transceiver solutions including ASSP and ASIC because the issue is related to the analog portion of the transceiver rather than the logic portion of the device.

Power consumption is a particular concern in chassis or backplane applications, where space is restricted so power or heat problems must be kept under control for devices to stay within operating range. The costs to implement adequate power management can be high. The techniques include:

- Heat sinks -which can greatly increase production costs.
- Expensive chassis design involving custom metalwork.
- Additional air flow involving the use of expensive fans. Additional cost introduced through additional maintenance once the systems are installed.
- Higher performance power supplies leading to extra component cost.

Stratix GX devices were designed with a low power PCML buffer to overcome some of the power problems within the transceiver. Each Quad (block of 4 Transceivers which can be aligned to produce a 10Gbps interface) requires 475 mW to operate at 3.125 Gbps across 40” of FR4 fabric. A single channel requires 175 mW per channel but that includes the overhead for all of the PMA section of the Quad. Additional channels require only 100mW. Stratix GX transceivers provide further power savings by allowing the transmitter or receiver to be disabled on a channel by channel basis. All these features have a considerable power saving when compared to other FPGA solutions and many ASIC/ASSP solutions, thus reducing overall system cost.

## Signal Integrity

FPGA with embedded transceiver are ideal for inter chip communications, whether across a backplane or for direct communication on a single card. Serial transceivers may be used to simplify a system by replacing a high speed parallel bus. At high speed, parallel busses can suffer from skew and crosstalk, making layout more complex. As the data rate increases the parallel bus width must increase to meet the data requirement and the problem worsens. In this case serial transceivers are extremely useful and provide the following advantages:

- Simpler board layout.
- Fewer components.
- Fewer PCB layer.

However the properties of high speed signaling, or moreover the edge speeds, mean that transmission line effects can make layout difficult. FR4 laminate material is widely used for PCB designs because it is generally a good conductive material and is cost effective.

Unfortunately, at high data rates the copper tracking on the material suffers from the “skin effect”, where high frequency signal tend to travel on the surface of the track, reducing the conductive area and increasing the signal attenuation.

A larger problem is caused by dielectric loss, which like skin effect causes the PCB material to act as a low pass filter and further attenuate the high frequency components from the signal. FR4 PCB material is particularly susceptible to dielectric loss and has a high dielectric tangent  $\tan(\delta)$ . Users can switch to an alternative PCB material such as GETEK which has a lower  $\tan(\delta)$ , or in other words is less lossy, but comes at additional costs.

Stratix GX includes extra functionality within the receiver to help overcome these issues, making design layout simpler and allowing the continued use of FR4 PCB fabric. More information on board layout can be found in the *Stratix GX board layout Guidelines*.

### *Programmable Drive Strength*

Transmission line losses can be overcome by increasing the drive strength of the differential pair to boost the signal seen by the receiver. The Stratix GX architecture allows the designer to select drive strength between 4mA and 16mA. The actual  $V_{od}$  setting is determined by the termination resistor value.

### *Pre-emphasis*

Issues associated with signal loss cannot always be solved by boosting the signal, as this will also boost any noise or jitter on the line and will result in greater power consumption. One solution is to use signal pre-emphasis, which effectively boosts the high frequency component of the transmitted signal by emphasizing the first data symbol after any signal transition.

Stratix GX provides programmable transmission pre-emphasis, allowing the user to select the level, depending on transmission medium and drive length. Figure 2a and 2b show the effect of 800mV signal with pre-emphasis at the transmitter (0") and at the receiver (20") operating at 3.125 Gbps.

Figure 2a.

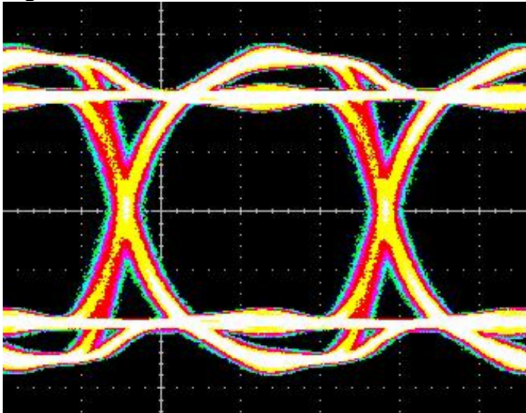
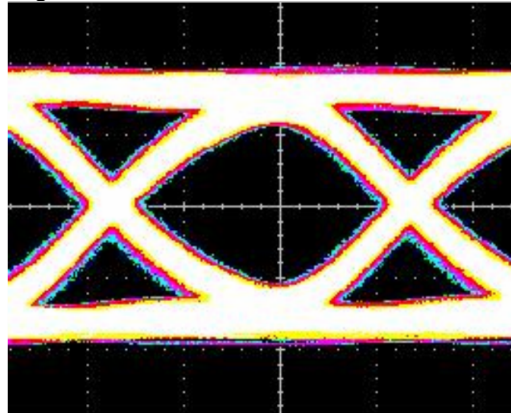


Figure 2b.



### *Receiver Equalization*

Pre-emphasis is a useful tool in overcoming transmission losses, but it can lead to greater power requirements, produce more Electro-Magnetic Interference (EMI) and make the system more susceptible to crosstalk. An alternative and more effective solution is to use Receiver equalization. In many applications it is possible to overcome the losses just by using Equalization and see better Bit Error performance. The receiver equalization provides circuitry that boosts the high frequency components of the signal at the receiver end to compensate for the transmission losses, while leaving the low frequency components untouched.

Stratix GX is unique as it is the only FPGA solution to offer Receiver equalization. This enables Stratix GX to interoperate with both ASIC and ASSP solutions over longer distances and in extremely poor operating conditions, where other solutions may fail. Stratix GX allows the user to configure the equalizer to operate at different track lengths. This ensures the system can be configured for its optimum performance. Figure 3 shows the SPICE simulated results of equalization. Figure 3a shows a simulated eye diagram into the receiver. Figure 3b shows the same signal after it has passed through receiver equalization.

Under certain operating conditions such as legacy systems not designed to support high speed transceivers or when interfacing to legacy devices, a combination of pre-emphasis and receiver equalization can provide an effective solution, where a single function may not solve the problem.

Figure 3a SPICE simulated input to Equalizer

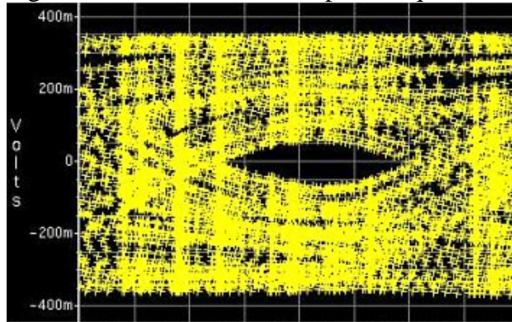
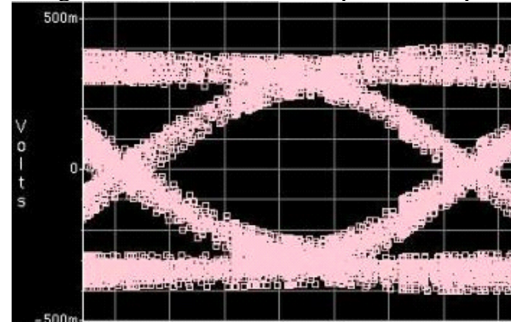


Fig 3b SPICE Simulated output from Equalizer



An important factor when considering a backplane design is transceiver drive capability; this is particularly an issue because the drive distance can be variable depending on backplane layout, number of slots in the backplane and the overall location of the master and slave cards. Many devices offer a drive capability of 20" which on the first sight would seem adequate because backplane systems do not tend to exceed 19" in length based on a typical 84HP chassis. However in reality, for a backplane that encompasses the whole of a chassis, a card in slot one interfacing to a card in slot twenty could easily exceed 30", if you consider stub lengths between the card and the backplane connector which are typically around 2" per card and the fact that it is extremely unlikely the track on the backplane will take the most direct route, particularly if it is end to end.

The signal integrity feature in Stratix GX enables the device to operate over 40" of FR4 PCB fabric. This allows Stratix GX to operate in the majority of backplane applications and conform to the form factor.

## Hot socketing

An important aspect of system based design is hot socketing capability. Hot socketing capability within High Speed Transceiver embedded FPGA's can be broken into two functions, Transceiver side and board or FPGA side. Both are important aspects for in-system hot swap support.

The transceiver side describes the ability to add or remove a transceiver channel without damaging it and without interrupting the other transceivers in the quad. This may, in the case of a line application, be a number of channels connected via cables, where one cable is removed without detrimental effects to the other channels. Alternatively in a backplane application, this could apply to a switch card connected to a number of line cards. In this case a line card may be removed from the system without causing a data loss between the switch card and the other line cards. Hot socketing capability is extremely important in many applications, but particularly in telecom applications because it allows for system maintenance or upgrade without any significant system down time.

FPGA hot socketing applies to the capability of the normal I/O to cope with the insertion or removal of the device from a system or chassis. This is again important in for a line card in a system, because it provides the ability to insert or remove a system or card from a backplane without damage and expect it to start up.

Stratix GX provides a solution for both transceiver and FPGA based hot socketing. Each transceiver is immune to the effects of the other transceivers being connected or disconnected. In addition the transceiver can be programmed to signal errors to the FPGA, such as a loss of lock signal from the Clock Recovery Unit when a connection is lost. The FPGA I/O within Stratix GX is designed to operate in a mixed signal environment and can tolerate any possible power up sequence. In effect this means that the Stratix GX I/O can be driven before or during a power up sequence without damage. The FPGA I/O is also designed not to

drive out during power up and prior to configuration, meaning a board can be inserted into a system without interfering with its operation.

## Self-Test

Self test of the transceiver and associated circuitry is an invaluable tool during the development and debug phase of a project. It allows the designer to test operation without the need to interface to external systems or devices. These techniques can also be used in the field for diagnosis. In order for self test to be useful, it is important that it has the ability to generate and detect codes or patterns in the transceiver. Self test modes must be flexible to enable test on different aspects of the transceiver.

Stratix GX provides a comprehensive self test solution. It provides the ability to perform both serial loop and parallel loop testing. Serial loop back tests the blocks within the serial data path by looping back between the output of the transmitter serializer and the receiver deserializer. Parallel loopback tests the circuitry within the parallel portion of the transceiver, looping from the transmitter synchronizer FIFO, through the 8b10b encoder and then back into the receiver FIFO via the 8b10b decoder, word aligner, pattern detector and rate matcher. A further parallel mode allows the user to bypass the 8b10b circuitry.

Stratix GX also includes two different pattern generators:

1. **BIST generator** and detector can be used to verify the entire transceiver by transmitting and receiving a set pattern via both serial and parallel loopback modes. The BIST generator can be programmed to generate a number of different test codes depending on the application.
2. **PRBS generator** and detector are used to generate and verify a PRBS pattern through the transceiver, supporting both serial and parallel modes. PRBS testing is particularly useful for performing Bit Error Rate testing and the Stratix GX device can be configured to generate a BIST flag if an error is recorded.

The self test modes enable full speed real time testing of the transceiver. In each case, test can be independent of the FPGA fabric, enabling the user to determine the suitability of the product without the need to generate the entire design.

## Source Synchronous Support

Many applications cannot rely on high speed transceivers to support applications and will therefore require some sort of high speed source synchronous (i.e. parallel) interface to provide data balance. Source Synchronous I/O describes an interface where clock and data are transmitted separately. As a link layer interface, Source Synchronous I/O can be used to move data from the transceiver into the rest of the system for processing. It is therefore important that the source synchronous I/O can support a sufficiently high data bandwidth to ensure the transceivers is permanently provisioned with data.

One example could be the SDH/SONET line card, where the line side of the interface would use high speed transceivers to support a 10Gbps interface, supporting the OC-192 specification; the backplane side of the interface could use an SPI4.2 as a bus interface across a backplane or interfacing to a network processor.

Another example would be high speed protocol which does not offer support for a CDR based transceiver. In this case, the interface will again be required to use a source synchronous interface.

In either case, source synchronous design is made difficult because of skew between clock and data or different data channels, making it difficult for the receiver to interpret the data and align it to the clock.

The Source Synchronous I/O elements provide by Stratix GX includes Design Phase Alignment (DPA) circuitry to overcome these issues. DPA operates by replicating the receiver clock signal into phases and then aligning the nearest clock phase to the incoming data. Once the data has been aligned to the clock it passes through a deserializer and can be byte aligned.

DPA enables the Source Synchronous interface on Stratix GX to operate at speeds up to 1Gbps. This superior data rate allows a higher bandwidth support to the transceiver interface. It also allows parallel standards such as SPI-4.2 and Parallel Rapid I/O to run at a higher data rate. This allows the interface to both support higher data rates and support further overheads for error correction and encryption.

For more information on the advantages of Dynamic Phase alignment refer to the document *Advantages of the Embedded DPA Circuitry in Stratix GX Devices*

## Protocol Advantages

### *XAUI*

One of the primary aims of the transceiver blocks within the Stratix GX architecture is to support the XAUI protocol. XAUI specification describes the interface between the Physical Coding Sublayer and the Media Access Controller for 10Gbit Ethernet standard. XAUI was conceived as an alternative to original the XGMII parallel interface and has been widely adopted for various applications including 10Gigabit Ethernet line cards, LAN to WAN bridges (SONET to Ethernet) and in particular as a protocol layer for backplane and chip to chip applications.

The XAUI protocol utilizes many of the functions used by other emerging protocols and is therefore an ideal base for a transceiver design. Stratix GX has embraced this protocol not only by meeting the electrical and jitter specifications but also by adding dedicated circuitry into the transceiver to make design implementation simpler. *AN249 Implementing 10 Gigabit Ethernet XAUI in Stratix GX devices* provides a full overview on how to use Stratix GX for XAUI applications. However it is worth mentioning one key feature supported by Stratix GX:

### *Channel Alignment*

The XAUI protocol requires 4 channels of 3.125Gbps data to support 10Gbps Ethernet (including 8B10B overhead). The XAUI protocol inserts a special alignment character (/A/) into the data to allow the receiver to detect the data and realign it.

The Stratix GX transceivers are provided as Quad interfaces, where 4 transceivers are aligned together. The Quads include dedicated alignment, routing and clocking circuitry to gain optimum performance and reduce latency. The internal alignment circuitry improves the efficiency within the FPGA, by removing the need to use external routing, which could interfere with both the transceiver performance and the general logic placements. This is particularly important because the alignment circuitry needs to meet tight time constraints in order to operate successfully

## SDH/SONET

The Stratix GX architecture is well suited to SDH/SONET protocol backplane applications. Whilst there is no standard protocol to support SDH/SONET backplane applications, many of the building functions used for line side applications can be implemented in backplane applications. Stratix GX transceiver technology provides a number of functions to support SDH/SONET based protocols.

- **Pattern Detection**      The Stratix GX transceiver includes a Pattern Detector to locate Frame Characters in the data stream. The pattern detector searches for A1A2 or A1A1A2A2 characters as specified in the OC standards. Once located, the pattern detector flags the word aligner to align the data into the pre transmitted data alignment. The dedicated circuitry prevents the need to use precious logic in the FPGA
- **Data Path**              Often FPGA solutions designed to support 8b10b encoded data do not offer flexibility in the data path back to the FPGA, should the encoder circuitry be bypassed. This is particularly applicable for protocols using 8 or 16 bit data because the transceiver may only be able to support the protocols by using circuitry within the FPGA to realign the data onto the correct word boundaries. Stratix GX has a flexible bus structure within the Transceiver which can provide support for 8, 10, 16 and 20 bit data between the transceiver and the FPGA, even when the 8b10b encoders are bypassed.
- **Clocking**                Stratix GX architecture provides flexible PLL's to support the high speed transceiver operation. The PLL's are granular, allowing for a number of different standards to be supported from a single clock source. This is particularly useful in SDH/SONET applications where a single clock source can be used to support clock rates between 622Mbps and 3.125Gbps. This will allow the same card to be used in a number of different applications.

For more information on how Stratix GX can be utilized in SDH/SONET applications refer to the document *Using Stratix GX for SONET/SDH backplane* white paper.

## SPI 4.2

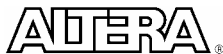
Primarily used in OC-192 systems, the SPI-4.2 standard interfaces cell and packet transfers at 10-Gbps between physical (PHY) and link layer devices. Due to layout issues discussed earlier in this document, SPI-4.2 utilizes source synchronous data transfer and is therefore restricted to around 800mbps using conventional I/O standards. However by using the DPA feature in Stratix GX, the interface can support data rates of 1Gbps.

Depending on the use of the interface in the application, the operational speed of SPI4.2 can vary. Though, if the interface is used on the system side, it tends to operate at higher data rates. This ensures the data from a network processor is constantly available at framer to ensure no idle packets in the transmission pipe. For this reason, the latest 10Gbps network processors tend to support 1Gbps interfaces.

For more information about the advantages of Stratix GX for the SPI-4.2 protocol refer to the document *Advantages of the Embedded DPA Circuitry in Stratix GX Devices*

## Conclusion

The demand for high speed transceivers is increasing as more applications need to support higher data bandwidths. Many new protocols are springing up to meet these challenges. There is now a real need for flexible transceiver architecture to meet these needs. By integrating high-speed serial transceiver into the high-performance Stratix architecture, the Stratix GX family provides a total solution for many different applications. Transceiver technology has been carefully implemented to provide full functionality, while also providing the flexibility to support modifications as these new protocols merge and change. The transceiver's properties, coupled with its low power requirement make it ideally suited to not just backplane but also chip to chip and other aspects of transceiver design.



101 Innovation Drive  
San Jose, CA 95134  
(408) 544-7000  
[www.altera.com](http://www.altera.com)

Copyright © 2003 Altera Corporation. All rights reserved. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations, and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries.\* All other product or service names are the property of their respective holders. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.