White Paper

MAX Series Configuration Controller using Flash Memory

Configuration bit stream sizes are increasing with the introduction of higher-density FPGAs. This increase requires more configuration devices to store the data and configure these FPGAs. As an alternative to using additional configuration devices, designers can use flash memory to store configuration data. To use flash memory and perform configuration, designers must use a flash memory configuration controller. By using the flash memory configuration controller, designers can also implement a remote system upgrade configuration scheme in their design. This white paper shows how to implement the flash memory controller in MAX® II, MAX 3000A, or MAX 7000 devices.

Configuration Controller Features

Designers can use the MAX series configuration controller for the following functions:

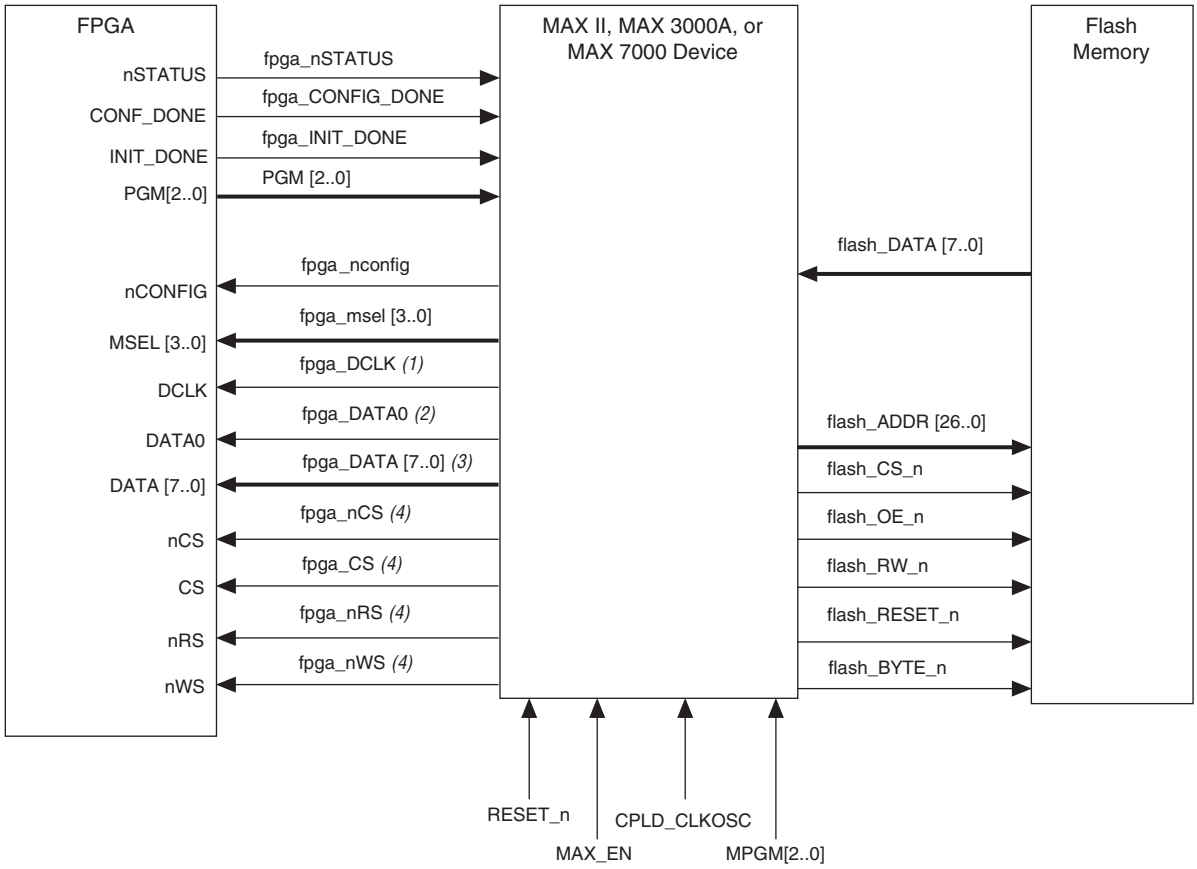
- Read configuration data from a flash memory.
- Configure Altera® FPGAs.
- Remote System Upgrade Configuration (only in Stratix® series FPGAs).
- Configuration from multiple pages of configuration data. MPGM pins allow designers to choose one of the configuration pages to configure FPGAs.

The MAX series configuration controller supports the following configuration schemes:

- Fast Passive Parallel (FPP) Mode (with and without decompression).
- Passive Serial (PS) Mode (with and without decompression).
- Passive Parallel Asynchronous (PPA) Mode.
- Remote System Upgrade (only in Stratix series FPGAs).

Figure 1 shows the flash memory controller block diagram.

Figure 1. Flash Memory Configuration Controller Block Diagram



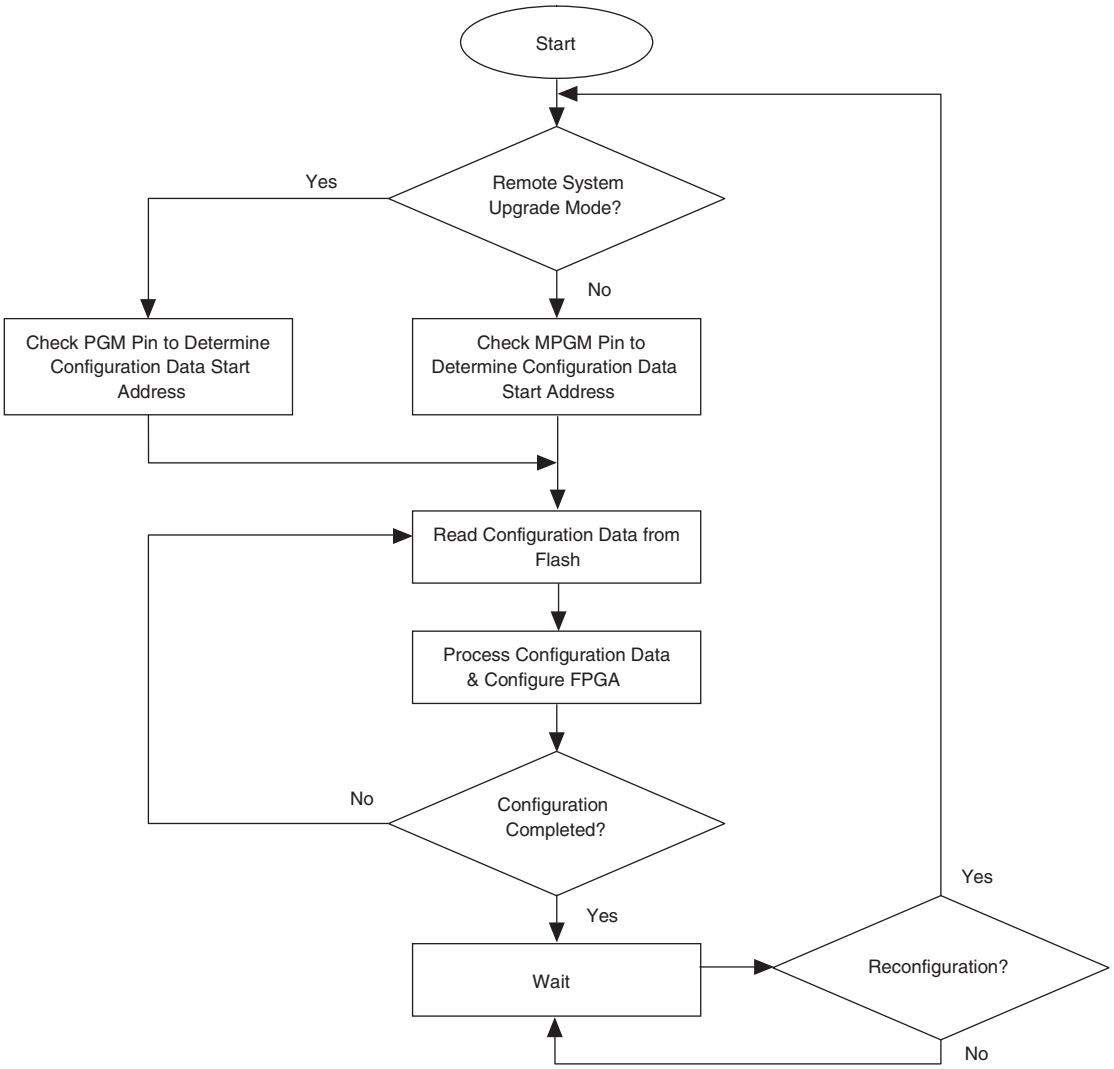
Notes to Figure 1:

(1) Not used in PPA mode.
(2) Not used in FPP or PPA mode.
(3) Not used in PS mode.
(4) Not use in PS or FPP mode.

Configuration Controller Operation

Figure 2 shows how the configuration controller executes the basic operation when it is powered up.

Figure 2. Flash Memory Configuration Controller Basic Operation Flow Chart



Page Selection for Configuration Controller

Flash memory can store multiple configuration pages in different addresses. The configuration controller allows the designer to select which configuration page in the flash memory to load during the configuration.

To determine which page to load, the controller reads the MPGM pin in non-remote upgrade mode or reads the PGM pin in remote upgrade mode. A Stratix series FPGA controls the PGM pins through the FPGA's remote system upgrade block. Designers can control MPGM pins using DIP switches or other devices.

Read & Process Configuration Data

The configuration controller reads configuration data through the flash_DATA [7..0] data bus. In PS mode, the configuration controller sends the serial configuration bit stream through the fpga_DATA0 pin. In FPP, FPP with decompression, and PPA mode, the configuration controller sends the configuration data through the fpga_DATA[7..0] data bus.

During the configuration process, the configuration controller executes the following process:

PS Mode

- Reads one byte (eight bits) of configuration data from flash and serializes the data
- Generates the DLCK signal and sends one bit of configuration data for every DLCK signal
- Reads the next byte of configuration data from flash memory after eight DLCK signals

FPP Mode

- Reads one byte (eight bits) of configuration data from flash
- Generates the DLCK signal and sends one byte (eight bits) of configuration data for every DLCK signal
- Reads the next byte of configuration data from flash memory after every DLCK signal

FPP Mode with Decompression

- Reads one byte (eight bits) of configuration data from flash
- Generates the DLCK signal and sends one byte (eight bits) of configuration data for every four DLCK signals
- Reads the next byte of configuration data on flash memory after every four DLCK signals

PPA Mode

- Reads one byte (eight bits) of configuration data from flash
- Sends one byte (eight bits) of configuration data to the FPGA and generates the control signals (nWS, nRS, CS, and nCS) to regulate the data transfer
- Reads the next byte of configuration data on flash memory after sending one byte of configuration data

For more information on the configuration scheme, refer to the *Configuration Handbook*.

Reconfiguration

The configuration controller reconfigures the FPGA if there is an error (nSTATUS goes low) during the configuration state.

The FPGA can initiate reconfiguration in remote update mode. The remote update block can update the PGM pin and initiate reconfiguration through the FPGA core_nconfig. The CONF_DONE pin goes low when the FPGA initiates core_nconfig in user mode. The configuration controller checks the CONF_DONE pin and reconfigures the FPGA after CONF_DONE goes low.

For more information about remote system upgrades, refer to the *Remote System Upgrades with Stratix II Devices* chapter of the *Stratix II Device Handbook* and the *Remote System Configuration with Stratix & Stratix GX Devices* chapter of the *Stratix Device Handbook*.

Configuration Scheme

The configuration controller supports the following configuration schemes:

- FPP Mode
- PS Mode
- PPA Mode
- Remote System Upgrade

FPP Mode

Stratix series devices and APEX™ II devices support the FPP configuration scheme. During FPP configuration, configuration data is transferred from a flash memory to the FPGA on the DATA[7..0] pins. This configuration data is latched into the FPGA on the rising edge of DCLK. Configuration data is transferred one byte per clock cycle for FPP without decompression and the design security feature. Configuration data is transferred one byte for every four clock cycles for FPP with decompression and the design security feature.

PS Mode

Stratix series devices, Cyclone™ series devices, APEX II, APEX 20K, Mercury™, ACEX® 1K, FLEX® 10K, and FLEX 6000 device families support the PS configuration scheme.

During PS configuration, configuration data is transferred from flash memory to the FPGA on the DATA (FLEX 6000 devices) or DATA0 (Stratix series, Cyclone series, or APEX II, APEX 20K, Mercury, ACEX 1K, and FLEX 10K devices) pin. This configuration data is latched into the FPGA on the rising edge of DCLK. Configuration data is transferred one bit per clock cycle.

PPA Mode

Stratix series devices, APEX II, APEX 20K, Mercury, ACEX 1K, and FLEX 10K device families support the PPA configuration scheme. During PPA configuration, configuration data is transferred from a storage device, such as a configuration device or flash memory to the FPGA on DATA[7..0] pins. Since this configuration scheme is asynchronous, control signals (nWS, nRS, CS, and nCS) regulate the configuration cycle.

For more information on the configuration scheme, refer to the *Configuration Handbook*.

Remote System Upgrade

The flash memory configuration controller supports remote system upgrade using FPP, PS, or PPA configuration modes to configure Stratix series FPGAs. The configuration controller determines which page to load in remote system upgrade mode by reading the PGM pin on the FPGA. The configuration controller monitors the nSTATUS pin to detect any error during configuration or to initiate reconfiguration after configuration mode. The Stratix series device remote system upgrade block initiates re-configuration to change the page.

For more information about remote system upgrades, refer to the *Remote System Upgrades with Stratix II Devices* chapter of the *Stratix II Device Handbook* and the *Remote System Configuration with Stratix & Stratix GX Devices* chapter of the *Stratix Device Handbook*.

Flash Memory

Designers must convert the configuration data from SRAM Object Files (**.sof**) into a HEXOUT file (**.hex** or **.hexout**) and program it into the flash memory. Designers can generate HEXOUT files by choosing the **Convert Programming Files** (Quartus II file menu).

For information on the HEXOUT file format, refer to the *Intel Hexadecimal Object File Format Specification*, available from Intel Corporation.

Designers can program flash memory prior to being placed on a board with standard programming equipment or in-system using test equipment. Since different flash memories have different algorithms, read the flash memory data sheet for programming information.

Source Code

The configuration controller reference design source code is available in Verilog HDL and VHDL code. The same source code can be compiled into the following four versions to support different configuration modes:

- FPP
- FPP Decompression
- PS
- PPA

The configuration controller reference design source code is written for MAX II, MAX 3000A, and MAX 7000 devices. The code reads from the AMD flash memory (AM29LV128) and configures the Stratix II device. Designers can customize and modify the code according to other hardware requirements.

Refer to the readme file attached with the source code for more details at **www.altera.com/literature/wp/wp_max_flash.zip**.

Conclusion

The flash memory configuration controller provides an alternative configuration solution for a design that uses high-density FPGAs. It offers the flexibility to use a bigger flash memory to store more configuration data. Designers can use this reference design to design remote upgrade systems for Stratix series FPGAs in FPP, PS, and PPA modes.

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