



FEATURES

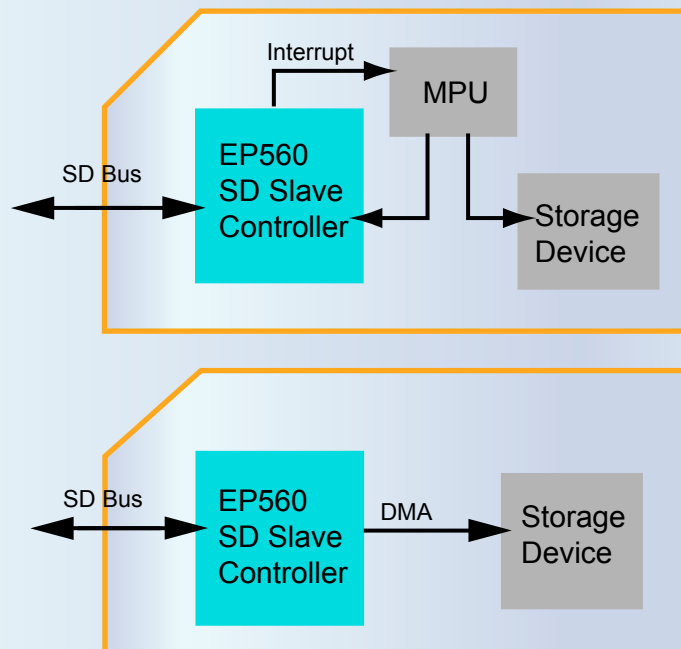
- Compatible with SD/SDIO specification 2.0 with 1 and 4 bit data transfer.
- Supports SD, SPI, SD combo card, and optional 8-bit MMC bus protocol.
- Supports both standard capacity and high capacity (SDHC) memory cards.
- High speed mode up to 50Mbyte/sec transfer rate.
- Simple 32-bit master interface to DMA data into user memory space.
- Optional interrupt-based transfer and separate user clock domain.
- Selectable maximum block size from 512 to 16Kbytes.
- Process most commands automatically without help from user logic.
- Contains SD and MMC standard slave register set.
- Supports multi-function SDIO and comb card, suspend, resume and read wait.
- Choice of user interface bus including AHB, APB, Wishbone, SH4, Avalon bus.

The EP560 SD Slave Controller IP core provides the simplest way to design a Secure Digital (SD) or MultiMedia Card (MMC) device. It serves as a bridge between the SD bus and user's application logic inside the card. It contains many flexible design features that allows it to be easily integrated to any card applications. It supports SD memory, SDIO, SDHC, MMC and combo card functions.

The EP560 SD slave controller processes all the bus request from the SD bus locally. It contains the standard card register set and state machines so that most request from the host are handled automatically without support from the user logic. This frees the application logic from the SD protocol constraints. Only data access are forwarded to user's application logic as read/write request. The IP core can be configured to operate as a DMA engine to access user logic or as a slave to the local MPU through request interrupt.

Configurations

The EP560 can be used in DMA mode to access user logic directly or in interrupt mode for request service from user's local micro-controller.





Other IP Cores

- SD Host Controller
- SD Development Kit
- CompactFlash ctrlr
- NAND Flash controller
- DMA Controller
- SDRAM controller
- PCI Bridge
- PCI Express
- AHB Bus Interface
- PowerPC Bus Interface

Deliverable

- Verilog or VHDL RTL code
- FPGA netlist: supported FPGA including Altera, Xilinx, Lattice and Actel
- Source code license includes test bench and simulation models.
- Synthesis script
- FPGA netlist includes routing and timing constraint file
- Top level design template
- Free source code for bus driver development

Flexibility

- EP560 user can choose from a rich set of features to suit each application requirement.
- CPU bus interface: AHB, APB, Wishbone, SH4, Avalon, generic.
- DMA mode and Interrupt mode.
- Separate clock domain for user interface from SD clock.
- SD memory, SDIO, Combo or MMC support.

The Eureka Advantage

Eureka Technology has been a leading silicon IP core provider since 1996. The company is based in Silicon Valley, California and has strong world-wide customer base. Since Eureka focuses exclusively in IP core development, high quality and high performance IP cores is the cornerstone to our success.

- Silicon proven with over 12 years of track records
- Source code and development kit available
- Simple licensing method
- Customization available

Eureka Technology Inc.
4962 El Camino Real, #108
Los Altos, CA 94022 USA
Tel: 1 650 960 3800
<http://www.eurekatech.com>
email: info@eurekatech.com

Please contact Eureka Technology for technical data sheet and pricing information.