

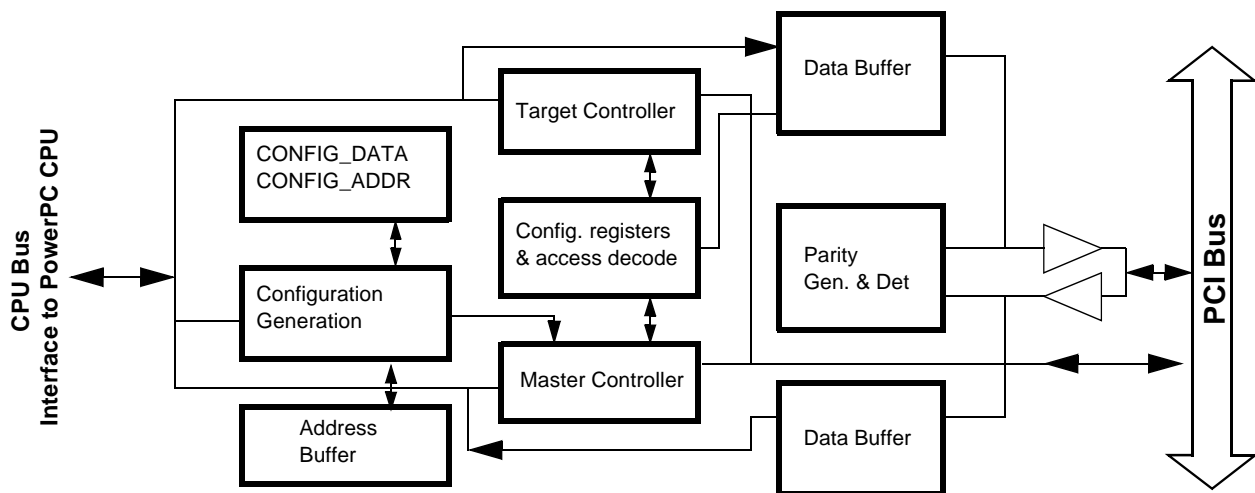


# EP433/434 PowerPC-PCI Bridge

## Product Summary

### FEATURES

- Fully supports PCI specification 2.1 and 2.2 protocol.
- Designed for ASIC and PLD implementations.
- Fully static design with edge triggered flip-flops.
- Supports all PowerPC CPU with 603 bus interface and MPC860 interface.
- Host bridge design includes bus master, bus target and central system functions.
- Generates standard PCI type 0 and type 1 configuration accesses.
- Combined bus master and target functions.
  - Master function
    - Initiate PCI memory and IO read/write.
    - Automatic transfer restart on target retry and disconnect
  - Target function
    - Memory or IO read/write
    - Configuration read/write
    - Support for back-end initiated target retry, disconnect and abort.
- Supports Zero wait state and user inserted wait state burst data transfer.
- Dual write buffer supports write data posting.
- User controlled burst and non-burst data transfer.
- Automatic handling of configuration register read/write access.
- Supports user initiated target retry, disconnect, abort and delayed transaction.
- Parity generation and parity error detection.
- Includes all PCI specific configuration registers.
- Supports high speed bus request and bus parking.
- Optional PCI bus arbiter with fix, rotating, and custom priority.





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### DESCRIPTION

The 32-bit PCI host bridge is designed for interfacing the PowerPC CPU with the PCI bus. This core contains options to support 32-bit or 64-bit back-end bus for different PowerPC CPUs. The host bridge consists of three functions: bus master, bus target and configuration access generation.

Other bus mastering devices on the PowerPC bus can also access the bridge. The core utilizes double data buffer design approach which minimizes design gate count and achieve highest possible data bandwidth at the same time.

The host bridge core allows the CPU or user logic to initialize the entire system during power-up reset. Configuration Mechanism #1 as defined by the PCI specification is implemented by the host bridge, and both type zero and type one transactions are supported. The local bus CPU requests configuration access on the PCI bus by writing to or reading from the CONFIG\_ADDR and CONFIG\_DATA registers which are contained in the host bridge. The location of these registers can be specified by the user. The host bridge initiates configuration read or write transaction to the target device as specified in CFG\_ADDR.

The PCI host bridge is capable of initiating memory or IO read and write upon back-end requests. The type of command and the burst size are specified by the user for each data transaction. Burst size can be pre-determined by the user for each transaction or changed as the transaction progresses.

Once a master transfer begins, the core monitors the target device's signals on the PCI bus and transfers data to the user logic. All different types of transfer termination are handled by the core. If a transfer is retried or disconnected by the target, the master core re-starts the transfer automatically without the assistance of the user logic. Bus request, bus parking, parity detection and generation all are handled by the core.

The PCI target controller is capable of handling memory and IO accesses on the PCI. All seven types of PCI memory/IO accesses are supported. Configuration register read and write transactions are supported locally by the bus target without assistance from the user logic. Data parity detection and generation are also handled by the core locally.

When a bus master on the PCI bus initiates a PCI transaction, the core decodes the address and the command and claims the transaction if the address is decoded to be within the address space defined in the base address register. The PCI transaction is propagated to the proper target device in simple protocol through the back-end bus.

The user interface allows the user to control the characteristics of the access. For example, the user can insert a wait state or transfer data without wait state according to its data bandwidth. Single or burst transfer, retry, disconnect, delay transac-



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tion and target abort can all be controlled by user logic.

The PCI target controller also responds to configuration read and write operations. The PCI configuration registers for the host bridge's own master and target functions are provided by the core and they can be accessed in the same way the host bridge accesses the configuration registers of other PCI devices. When a configuration request targets the host bridge's own configuration register, the host bridge functions as both the master and target for the configuration cycle on the PCI bus.

The following table summarizes the optional features which are provided with the core as required by user application.

Options	Description
CPU bus size	32-bit or 64-bit CPU interface
Unidirectional host bridge	Remove target function support to minimize gate count.
CPU type	The EP433 supports PowerPC CPU with 603 bus interface such as 603, 604, 740, and 750. The EP434 supports PowerPC MPC860. Other variation of the 603 bus such as the MPC8260 and 7400 are supported.
Target back-end	Request received by the PCI target can be directed to a separate memory interface or to the CPU interface.
Bus arbiter	Arbitration for the PCI bus and/or CPU bus.
Base address registers	Supports multiple base address registers, memory or IO mapped, and expansion ROM base address register.
Target burst	Single transfer support available to minimize core size.
Asynchronous clock domains	Separate and asynchronous user and PCI clock domains. The core provides re-synchronization and data FIFO.