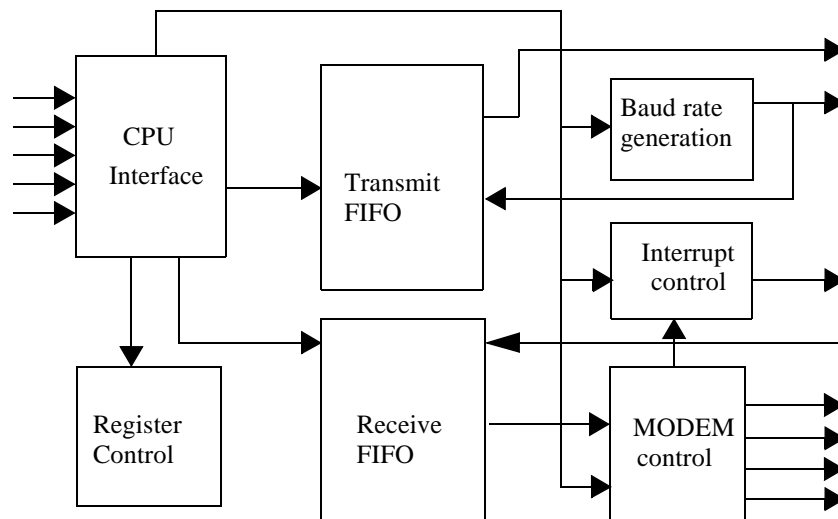




Product Summary

FEATURES

- Functionally compatible with 16550.
- Supports Character (16450) and FIFO (16550) mode operations.
- Designed optimized for ASIC and PLD implementations.
- Synchronous design with edge triggered flip-flops based on system clock input.
- 16-byte FIFO for transmitter and receiver reduces the number of interrupt to the CPU.
- Holding register in non-FIFO mode eliminates the need for precise synchronization between the CPU and UART.
- Add or deletes standard asynchronous communication bits (start, stop, and parity) to or from the serial data.
- Independently controlled transmit, receive, line status and data set interrupts.
- Programmable baud generator divides input clock by 2 to $(2^{16}-1)$ and generates the 16X clock.
- Synchronous input sampling timed by internal receiver clock.
- MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD).
- Programmable features: 5 to 8 bit characters, even/odd parities and no parity, 1, 1.5 and 2 stop bits, programmable baud rate.
- False start bit detection.
- Complete status reporting capabilities.
- Line break generation and detection.
- Internal Loopback.





DESCRIPTIONS

The UART performs serial-to-parallel conversion on data received from a peripheral device or a MODEM, and parallel-to-serial conversion on data received from the CPU. The EP600 supports both the character mode (16450) and FIFO mode (16550) of operations. Default operation is character mode so that upon power up, the UART is compatible with 16450. When the FIFO mode is activated, it allows 16 bytes of data to be stored for receive or transmit data.

Status and command to the UART can be accessed by the CPU through the access port. All the control of the UART are done through the access port.

The UART includes a baud rate generator which can be programmed to different timing based on the system clock. The programming range is from 2 to $2^{16}-1$ clocks.

Different types of interrupt generation are supported by the UART. The interrupt can be customized to user's requirement to minimize computing requirement for the CPU.