

1 Introduction

Ethernet is available in different speeds (10/100/1000 and 10000Mbps) and provides connectivity to meet a wide range of needs from desktop to switches. MorethanIP IP solutions provide a solution for each Ethernet application with a library of configurable MAC (Media Access Control) and PCS (Physical Coding Sub-layer) Cores.

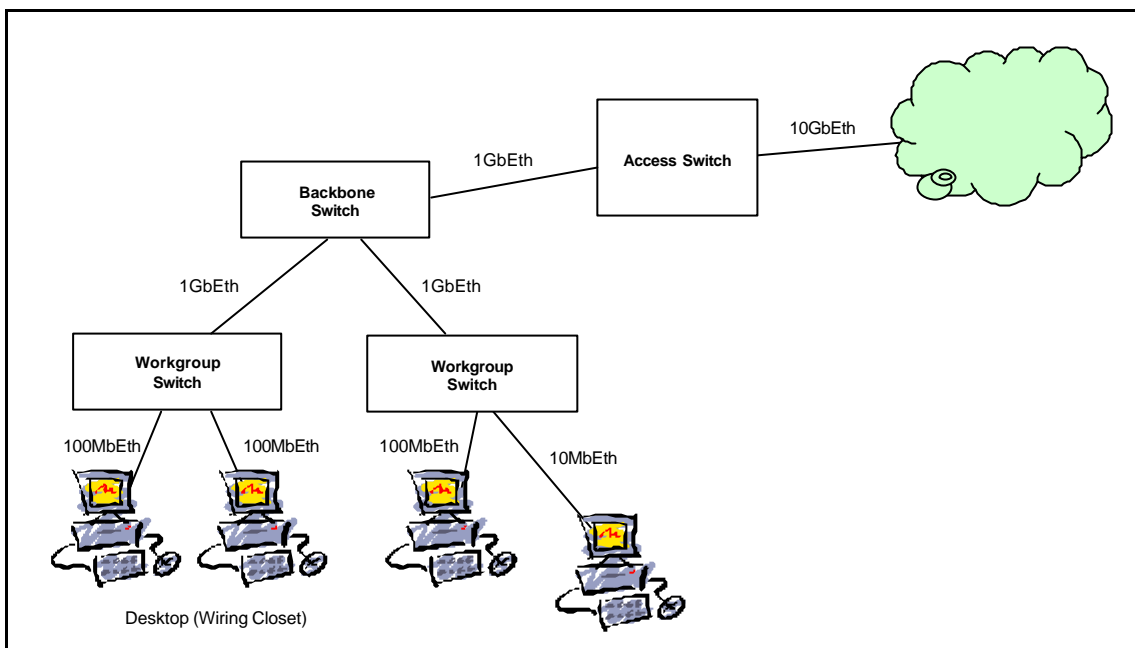


Figure 1: Enterprise LAN Topology Example

The programmable 10/100 Ethernet MAC from MorethanIP provides, with a single IP Core, a solution for Ethernet applications (Line Card, NIC card or switching) operating at 10 or 100 Mbps. The 10/100 MAC Core operates in Full- or Half-Duplex mode, supports transparent (For switching applications) and full Ethernet frame termination / generation (For NIC or line cards applications).

The core can seamlessly connect to any industry standard Ethernet PHY device through the Media Independent Interface (MII) and to a user application via the Avalon SOC (System on a Chip) bus interface which provides seamless connectivity to any Avalon based system.

The core is optionally delivered in generic synthesizable HDL code (For use in Altera CPLD or ASIC technologies), or as a CPLD netlist, which provides a lower cost solution.

The MAC is fully integrated in the Altera SOPC builder for easy system integration and use. It includes supporting files for software development and drivers for the *Plugs* TCP/IP stack library.

2 Application Example

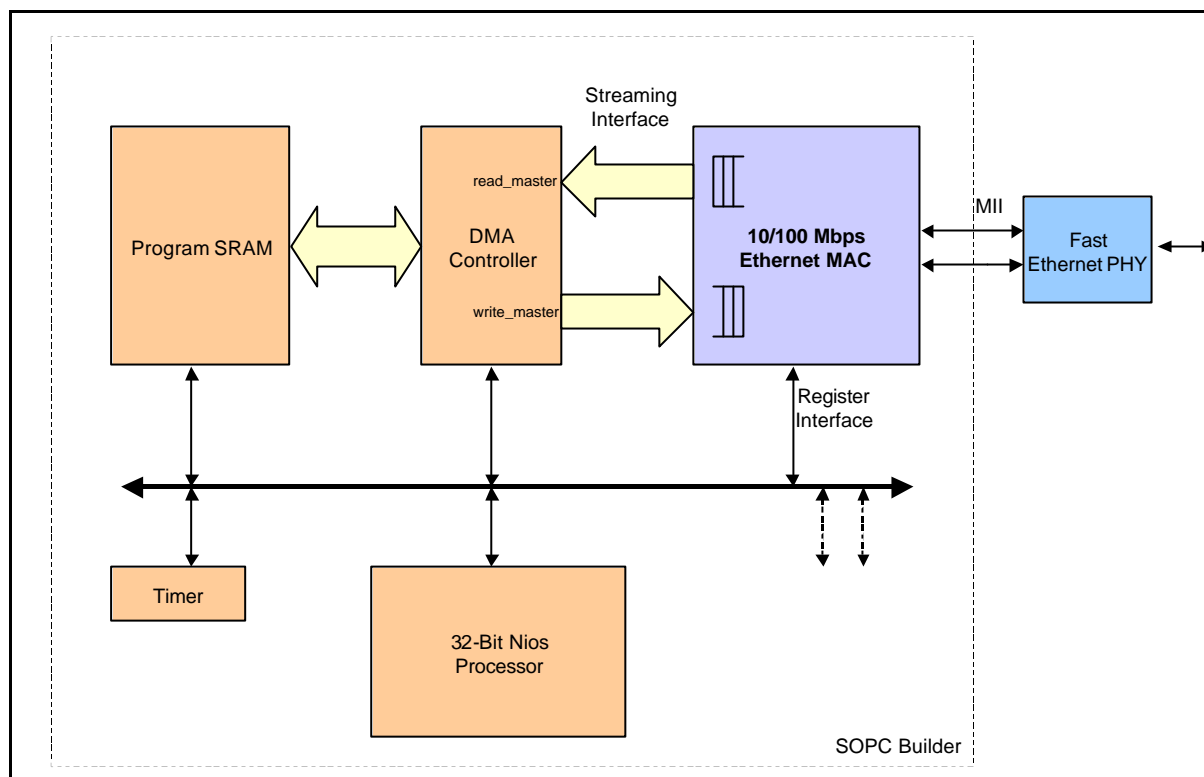


Figure 2: Application Example

3 10/100 Mbps Ethernet MAC core Features

- Implements the full 802.3 specification with preamble / SFD generation, frame padding generation, CRC generation and checking on transmit and receive respectively
- Dynamically configurable to support 10Mbps, 100Mbps or Gigabit operation
- Supports, for 10/100Mbps operation, full duplex or half duplex operation selectable via a Core configuration options
- Supports AMD Magic Packet detection with interrupt on receive
- Seamless interface to commercial Fast Ethernet PHY device via a 4-Bit Medium Independent Interface (MII) operating at 25MHz
- Other Medium Independent Interfaces (e.g. RGMII, RMII,...) optionally available, contact MorethanIP for info
- Avalon System Interface with separate slave ports for data and control
- Avalon data path ports with full streaming support allowing efficient DMA transactions
- Supports any type of Ethernet Frames such as SNAP / LLC or IP traffic
- Supports Unicast, Multicast and Broadcast Ethernet frames
- CRC-32 checking at full speed with optional forwarding of the FCS field to the user application
- CRC-32 generation and append on transmit or forwarding of user application provided FCS selectable on a per-frame basis

Product Brief

Version 3.3 - November 2003

- When operating in Full Duplex mode, implements fully automated Pause Frame (802.3 Annex 31A) generation and termination providing flow control without user application intervention
- When operating in full duplex mode, pause quanta used to form Pause frames, dynamically programmable
- Pause frame generation additionally controllable by user application offering flexible traffic flow control
- Optional forwarding of received pause frames to the user application when operating in Full Duplex mode
- In half-duplex mode, provides full collision support, including jamming, backoff, and automatic retransmission
- Support for VLAN tagged frames according to IEEE 802.1Q
- Programmable node Unicast MAC address with insertion on transmit and frame filtering on receive
- Optional up to four supplemental MAC addresses to filter unicast traffic from up to 5 different MAC addresses
- Programmable Promiscuous mode support to accept all Unicast MAC frame regardless of their destination MAC address
- Multicast address filtering on receive based on 64 entries hash table reducing higher layer processing load
- Programmable frame maximum length providing support for any standard or proprietary frame length (e.g. 9K-Bytes Jumbo Frames)
- Statistic indicators provide support for IEEE 802.3 basic and mandatory Management Information Database (MIB) package, Ethernet MIB (RFC 2665) and Remote Network Monitoring (RFC 2819) enabling implementation in SNMP management environments
- Includes data path FIFOs with fully programmable depth and threshold levels ensuring data rates of 1Gbps with full back-to-back frame transfer support
- Data path FIFOs with clock rate decoupling between Avalon and Line clocks
- Separate status word available for each received frame on the user interface providing information such as frame length, frame type and error information
- MDIO Master interface for PHY device configuration and management with two programmable MDIO base addresses and memory-mapped access
- Available for CPLD or ASIC implementation
- Fully integrated in Altera SOPC Builder for ease of use and instant system generation
- C Language Software Drivers and example programs
- Drivers provided for TCP/IP *Plugs* library

4 MAC Core Block Diagram

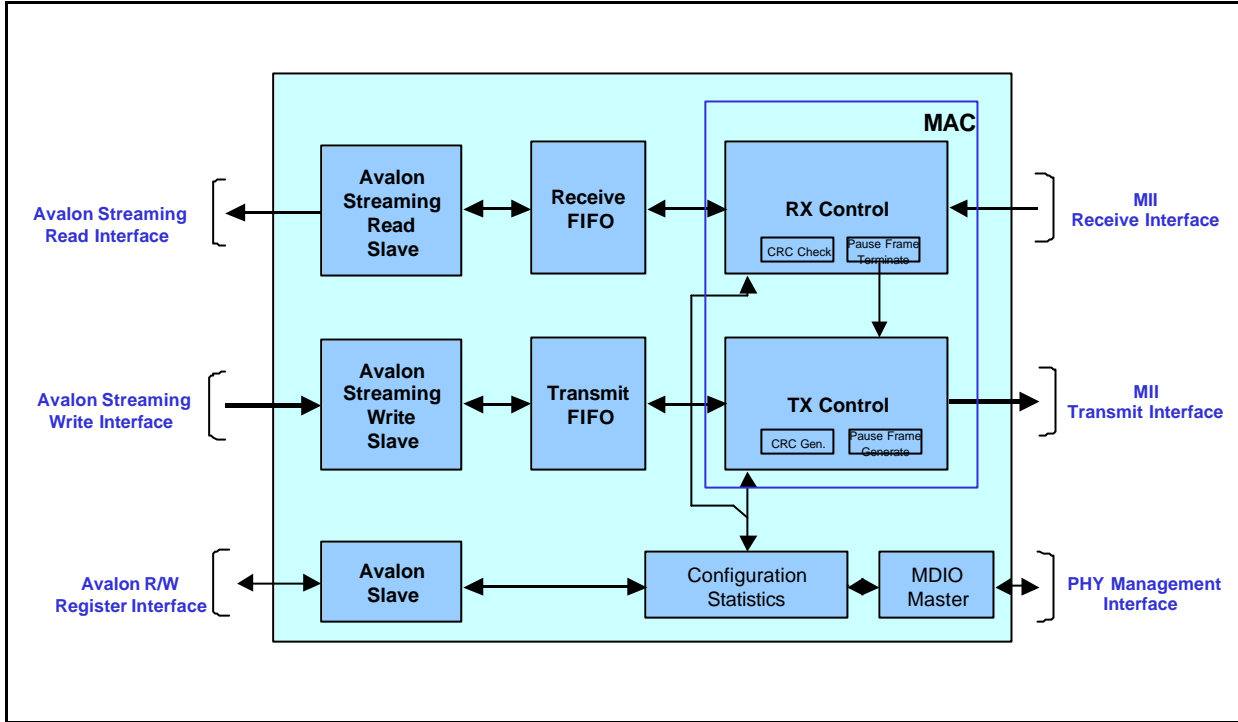


Figure 3: 10/100Mbps Ethernet MAC with Avalon Interface Core Overview

5 Implementation Summary

5.1 MAC Core with Avalon Bus Interface

Table 1: 10/100 Ethernet MAC Complexity Summary

Target Device Family	Speed Grade	Complexity (With 2048 Byte FIFO per direction)		Performance
		LEs	RAM bits	
APEX20KE	-2	4200	54080	50 MHz
STRATIX	-7	4100	54080	130 MHz
CYCLONE	-8	4100	54080	130MHz

6 10/100Mbps Ethernet MAC Design Kit Overview

Table 2: Design Kit Overview

<i>Design and Simulation</i>	
Language	Optimized VHDL / Verilog or lower cost CPLD encrypted netlist.
Simulation	Configurable VHDL / Verilog Testbench with embedded frame generator and checker providing an easy to use and robust de-bugging environment.
Verification	Comprehensive test environment with Ethernet frame generator and verification models for standard compliant and errored frame generation and automated core behavior verification.
<i>Supported Design Tools</i>	
Simulation	Modelsim Version 5.6a or higher.
Synthesis	Exemplar 2002d or higher.
Implementation	Quartus II V2.2 or Higher, SOPC Builder 2.8 or higher

7 References

1. IEEE 802.3 2000 Edition
2. IEEE 802.1Q 1998 Edition
3. RFC2665, Definitions of Managed Objects for the Ethernet-like Interface Type, www.ietf.org
4. RFC2863, The interfaces Group MIB, www.ietf.org

8 Ordering Code

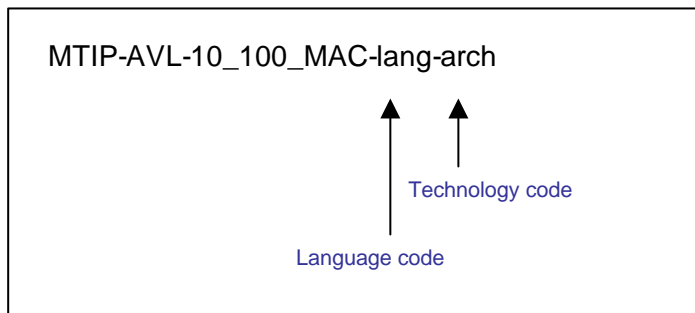


Table 3: Language Code

Technology Code	Target Technology
BIN	Encrypted CPLD netlist.
VHDL	Synthesizable generic VHDL source code for CPLD or ASIC implementations
VLOG	Synthesizable generic Verilog source code for CPLD or ASIC implementations

Table 4: Technology Code

Technology Code	Target Technology
GEN	Source code option for Altera CPLDs (APEX20KE, CYCLONE, APEX-II, STRATIX or STRATIX GX) or ASIC implementations.
ALTR	Encrypted netlist for Altera CPLDs (APEX20KE, APEX-II, CYCLONE, STRATIX or STRATIX GX).

9 Contact

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