

**Introduction**

Ethernet is available in different speeds (10/100/1000 and 10000Mbps) and provides connectivity to meet a wide range of needs and from desktop to switches. MorethanIP IP solutions provide a solution for each Ethernet application with a library of configurable MAC (Medium Access Control) and PCS (Physical Coding Sub-layer) Cores.

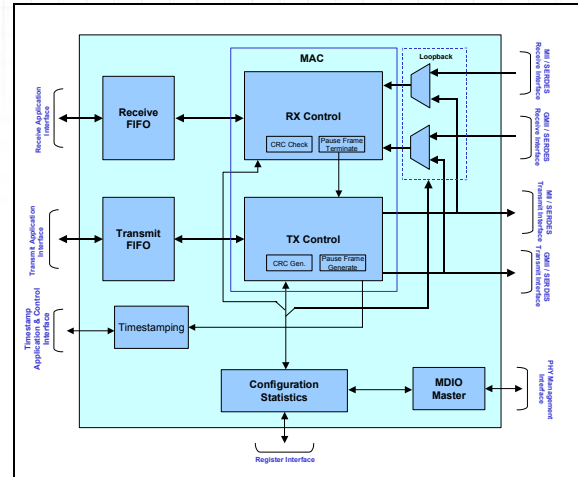
For industrial automation application the IEEE 1588 standard is becoming the main technology for precise time synchronization on Ethernet networks providing accurate clock synchronization for distributed control nodes to overcome one of the drawbacks of Ethernet.

The programmable 10/100/100 Ethernet MAC with IEEE 1588 support from MorethanIP integrates a standard IEEE 802.3 Ethernet MAC with a time stamping module to support Ethernet applications requiring precise timing references for incoming and outgoing frames to implement a distributed time synchronization protocol such as the IEEE 1588.

The 10/100/1000 MAC can also be used in conjunction with the MorethanIP TCP/IP acceleration engine to provide an efficient and compact solution to deliver high bandwidth to client applications.

The core can be seamlessly connected to any industry standard Gigabit Ethernet PHY device via a Gigabit Medium Independent Interface (GMII for 1000Mbps application) or Medium Independent Interface (MII for 10/100Mbps applications) and to a user application via a SOC (System on a Chip) interface which provides seamless connectivity to any MorethanIP core interfaces or any third party module which implements an interface compatible with the Altera Atlantic specification.

The core is optionally delivered in generic synthesizable HDL code (For use in FPGA or ASIC technologies), or as a FPGA encrypted source format.



**DPE-1588 Controller Block Diagram**

**1588 Tri-Speed Ethernet MAC Key Features**

- Implements two independent Triple Speed 10/100/1000Mbps Ethernet MACs
- Preamble and SFD (Start of Frame delimiter) insertion and deletion
- Optional Padding termination/insertion for NIC applications or forwarding of unmodified frames for switching applications
- Support for VLAN tagged frames according to IEEE 802.1Q specification in both transmit and receive
- CRC-32 checking at full speed using a multi-stage CRC calculation architecture with optional forwarding of the FCS field to the user application
- CRC-32 generation and append on transmit or forwarding of user application provided FCS selectable on a per-frame basis
- Per Channel Individual Unicast MAC address for frame filtering or fully transparent operation
- Programmable frame length to support standard and proprietary frame lengths
- Embedded programmable Multicast address resolution hash table
- Programmable Half Duplex out Full Duplex network operation (10/100Mbps)
- Half Duplex collision and automatic frame re-transmission with Jamming and Back-Off timer
- In Full Duplex, optional automatic Pause Frame generation from programmable FIFO congestion thresholds or by dedicated command pin with programmable Quanta
- Per Channel programmable Automatic Xon and Xoff flow control frame generations

- Implements per channel a 8K bytes FIFOs on the receive paths and a 2K byte FIFO on the transmit path
- Per Channel Network statistics

### IEEE 1588 Support

- Support for all IEEE 1588 Frames
- Reference Clock can be Chosen independently of the Network speed
- Software Programmable Precise Time-Stamping of Ingress Frames and Egress Frames
- Timer monitoring capabilities for System calibration and timing accuracy management
- Precise time stamping of external events with programmable interrupt generation
- Programmable event and interrupt generation for external system control
- Hardware and Software controllable timer synchronization

### Development Boards

- Standard Altera Cyclone II, Stratix and Stratix II FPGA Prototyping / Development Boards
- Comprehensive 10/100 and 10/100/1000 Ethernet PHY board Selection

### Implementation Summary

#### Altera FPGA Implementation Summary

	<i>Cyclone II</i>	<i>Stratix II</i>
<b>Speed Grade</b>	C8 / I8	C5 / --
<b>Complexity</b>	LEs	17,000 LEs <sup>(1)</sup>
<b>Performance</b>	130Mhz	160MHz
<b>Requirements</b>	125MHz	

1. The Logic Element count for Stratix II devices is based on the number of adaptive look-up tables (ALUTs) used for the design as reported by the Quartus II software.

### Contact

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