PLL Role in High-Speed Interfaces

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Agenda
- High-Speed Interface Clock Requirements
- Why High-Speed Interfaces Need Phase-Locked Loops ( PLLs )
- PLL Integration
- Jitter Issues
High-Speed Interface Clock
Requirements

<table>
<thead>
<tr>
<th>I/O Standard</th>
<th>Data Rate</th>
<th>Clock Speed</th>
<th>Clock Multiplication</th>
</tr>
</thead>
<tbody>
<tr>
<td>HyperTransport</td>
<td>1.6 Gbps</td>
<td>800 MHz</td>
<td>2</td>
</tr>
<tr>
<td>RapidIO</td>
<td>2.0 Gbps</td>
<td>1.0 GHz</td>
<td>2</td>
</tr>
<tr>
<td>POS-PHY 4</td>
<td>832 Mbps</td>
<td>416 MHz</td>
<td>2</td>
</tr>
<tr>
<td>SPI-4</td>
<td>622 Mbps</td>
<td>311 MHz</td>
<td>2</td>
</tr>
<tr>
<td>SFI-4</td>
<td>622 Mbps</td>
<td>622 MHz</td>
<td>1</td>
</tr>
<tr>
<td>UTOPIA IV</td>
<td>415 Mbps</td>
<td>415 MHz</td>
<td>1</td>
</tr>
</tbody>
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High-Speed I/O Interface

- High-Speed Interface Requires Clock Multiplication & Division
- Need To Limit Effect of Jitter
High-Speed I/O Interface

- Use PLL to Meet These Needs

Parallel-Serial Converter → 624-Mbit Data → Serial-Parallel Converter

System Logic

PLL Manages Clock within Devices

PLL Capabilities

- Clock Multiplication/Division

Input Clock 50 MHz

\[ F_{\text{out}} = \frac{F_{\text{in}} \times M}{N \times K} \]

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Other PLL Capabilities

- Zero-Delay Buffering
- Duty-Cycle Correction
- Phase Shifting
- Jitter Filtering

![PLL Circuit Diagram]

Embedded PLL Advantages

- Avoid Routing Multiple Clocks
- Avoid Crosstalk
- Enable Easy Frequency Synthesis

![Clock Source Diagrams]
What is Jitter?

- Short-Term Variation of Signal from Ideal Location
- Jitter Types
  - Period
  - Cycle-to-Cycle
  - Long-Term

Reference Signal

Jitter Types

- Period
- Cycle-to-Cycle
- Long-Term

Jitter Effects

- Jitter Can Shorten Effective Clock Cycle
- Short Clock Cycle Causes Incorrect Data Transfer

Data Input | D Q | Combinatorial Logic | D Q | Data Output

Clock Input

Clock Data

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When Is Jitter Critical?

- For Source-Synchronous Clocking:
  - Time Unit Interval (TUI)
  - Long TUI: Large RSKM, Jitter Less Critical
  - Short TUI: Small RSKM, Jitter Critical!

Data Rate & Jitter

- Low Jitter Required to Meet RSKM Specification
Jitter Classes

- Random
  - Probabilistic Timing Variations
  - Caused by Random Thermal Effects

- Deterministic
  - Repeatable Timing Variations
  - Caused by Specific Issues
    - e.g., Signal Modulation, Crosstalk

**Total Jitter = Random + Deterministic**

Jitter Transfer Definition

- Input Jitter May Be Reduced or Amplified
- Transfer Curve Shows Performance
  - > 0 dB: Amplification
  - < 0 dB: Reduction
- Deterministic & Random Jitter Transfer May Be Different
Deterministic Jitter Transfer

- PLL Can Reduce Deterministic Jitter
- Delay-Locked Loop (DLL) Amplifies Deterministic Jitter

![Jitter Transfer Graph]

- DJ Transfer
  - Input clk = 128 MHz; RMS Input Jitter = 45 ps

PLL Amplification: 77%

DLL Amplification: 44%

Random Jitter Transfer

- PLL Reduces Random Jitter

![Random Jitter Graph]
Jitter Summary

- Jitter Limits System Performance
- PLL Is De Facto Standard for Jitter Management
  - Searching www.arrow.com Finds:
    - 2 DLLs
    - 351 PLLs

PLL Summary

- High-Speed Interfaces Require PLLs
- Embedded PLLs Solve System Electrical Issues
- Manage Jitter to Ensure High System Performance