The Altera® Quartus® II design software provides a complete design environment that easily adapts to your specific design requirements. This handbook is arranged in chapters, sections, and volumes that correspond to the major stages in the overall design flow. For a general introduction to features and the standard design flow in the software, refer to the Introduction to the Quartus II Software manual.

This section is an introduction to design planning. It documents various specialized design flows in the following chapters:

- **Chapter 1, Design Planning with the Quartus II Software**
  This chapter is an overview of various design planning considerations: device selection, early power estimation, I/O pin planning, and design planning. To help you improve design productivity, it provides recommendations and describes various tools available for Altera FPGAs.

- **Chapter 2, Quartus II Incremental Compilation for Hierarchical and Team-Based Design**
  This chapter documents Altera’s incremental design and compilation flow, which allows you to preserve the results and performance for unchanged logic in your design as you make changes elsewhere, reduces design iteration time by up to 70% so you achieve timing closure efficiently, and facilitates modular hierarchical and team-based design flows using top-down or bottom-up methodologies.

- **Chapter 3, Designing HardCopy Series Devices**
  With the Quartus II software, you can use an FPGA device as a prototype and seamlessly migrate your design to a HardCopy ASIC to reduce cost for volume production. This chapter describes the Quartus II support for HardCopy design flows.

- **Chapter 4, Quartus II Design Separation Flow**
  This chapter describes rules and guidelines for creating a floorplan with the Design Separation flow. The Quartus II Design Separation flow provides the ability to design physically independent structures on a single device. This allows system designers to achieve a higher level of integration on a single FPGA, and alleviates increasingly strict Size Weight and Power (SWaP) requirements.